Core8051s v2.4 Release Notes

This is the production release for the Core8051s IP core. These release notes describe the features and enhancements for Core8051s v2.4. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Core8051s is a highly configurable processor that can be used to build compact and efficient microcontroller subsystems. To minimize area, the inbuilt 8051 peripherals are not present within the processor. The external SFR interface normally present on 8051 microcontrollers is replaced by an advanced peripheral bus (APB) v3.0 interface. This allows the user to decide which peripherals to add to the system.

Key Features

- Configurable 8-bit processor
- Can be targeted by 8051 C compilers, such as Keil or SDCC. SDCC is bundled with Actel's SoftConsole software development environment.
- Inbuilt 8051 peripherals such as timer, I/O ports, and serial channel are not included. APB peripherals can be optionally included.
- APB v3.0 interface on the processor for connecting to APB peripherals
- On-chip instrumentation (OCI) debug logic can be optionally included to facilitate JTAG based debugging.
- The internal 256x8 RAM within the processor can be implemented using RAM macro blocks or registers (FPGA tiles).
- Multiple configurable options for optimal implementation

Interfaces

Core8051s has a memory interface compatible with the memory interface of the earlier Core8051 core. This interface uses a shared bus to access external data memory and program memory. Core8051s also has an APB v3.0 interface for connecting to peripherals, and a debug interface that is used when the optional OCI debug logic is included. Additional individual ports are present on the core to facilitate clock, reset, and interrupt signals.

Note: CoreAPB3 is compatible with APB v3.0 and should be used to connect to the APB interface of Core8051s. CoreAPB should not be used with Core8051s because it does not support the PREADY and PSLVERR signals which were introduced in APB v3.0.

Documentation

This release contains a copy of the *Core8051s Handbook*, which describes the core functionality and how to use the core.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at http://www.actel.com.

Delivery Types

The Core8051s core is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Actel Libero® Integrated Design Environment (IDE). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core.

Supported Families

- IGLOO®/e/PLUS
- ProASIC3®/E/L
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S

Supported Tool Flows

This version should be used with Libero® Integrated Design Environment (IDE) v8.6 or higher.

Installation Instructions

Core8051s is available through the Libero IDE IP Catalog. It can be downloaded from a remote web-based repository and installed into the user's local vault, ready for use. Once installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

Release History

Table 1 provides the release history of Core8051s.

Table 1 • **Core8051s Release History**

Version	Date	Changes
2.4	September 10	Fixed bugs and issues as described in Table 2.
2.3	August 09	Added support for the following device families: IGLOO, IGLOOe, IGLOO PLUS, ProASIC3L, Axcelerator, and RTAX-S. Added IEN and ICON special function registers which provide interrupt enable and control bits for INT0 and INT1 interrupts. *Note: The interrupt enable bits in the IEN register are not set by default. If updating an instance of Core8051s to v2.3 within a system design that uses interrupts, the software running on the processor must be updated to enable the interrupts.* The USE_OCI and USE_UJTAG RTL parameters have been replaced by a single DEBUG parameter. *Note: If updating an instance of Core8051s to v2.3 within an existing SmartDesign design, error messages will appear in the Libero IDE Log window referring to USE_OCI and USE_UJTAG. These messages can be safely ignored.* Changed BFM command script syntax: waitirq and waitfiq commands have been replaced by waitint0 and waitint1. Fixed bugs and issues as described in Table 3 on page 4.
2.2	November 06	First production release

Resolved Issues in the v2.4 Release

Table 2 lists the software action requests (SARs) that were resolved in the Core8051s v2.4 release.

Table 2 • **Resolved Issues in the v2.4 Release**

SAR Number	Description
20643	Inferring of registers for internal 256x8 RAM now works correctly for obfuscated VHDL flow.
22428	The correct number of wait states is now inserted during the first instruction fetch when the processor has been configured to use a fixed number of wait states.

Resolved Issues in the v2.3 Release

Table 3 lists the software action requests (SARs) that were resolved in the Core8051s v2.3 release.

Table 3 • **Resolved Issues in the v2.3 Release**

SAR Number	Description
11722	Fixed problem with loading program memory via debugger when the MEMPSACKI acknowledge signal is used to control accesses to program memory.
11792	Fixed problem where writes to top 4 Kbytes of program memory resulted in writes to the APB interface.
11802 12904	Added support for more device families.
13032	Added interrupt enable and control bits (in IEN and ICON SFR registers) for INT0 and INT1 interrupts.

Known Limitations and Workarounds

There are no known limitations or workarounds in the Core8051s v2.4 release.

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