
Core429_APB v3.11 Release Notes

These release notes describe features and enhancements, and contain information about system requirements, supported families, implementations, and known issues and workarounds.

Key Features

Core429_APB is a highly configurable core with the following features:

- Supports ARINC specification 429-16
- Supports APB interface
- Configurable up to 16 Rx and 16 Tx channels
- Programmable FIFO depth
- Programmable interrupt generation
- Configurable label memory size
- Selectable data rate on each channel

Supported Interface

No standard interface available.

Delivery Types

The Core429_APB core is licensed in two ways: Obfuscated and register transfer level (RTL). Complete obfuscated RTL source code is provided for the core.

Supported Families

The following families are supported in this version:

- SmartFusion[®]2
- IGLOO[®]2
- IGLOO
- IGLOOe
- IGLOO PLUS
- ProASIC[®]3/E
- Fusion[®]
- SmartFusion
- Axcelerator[®]
- RTAX[™]-S
- ProASIC^{PLUS}[®]
- ProASIC[®]3
- ProASIC3L

Supported Tool Flows

Use Libero SoC v9.0 or later with Core429_APB release 3.11.

Installation Instructions

The Core429_APB CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Using DirectCore in Libero SoC User Guide](#) or [Libero SoC online help](#) for further instructions on core installation, licensing, and general use.

Documentation

This release contains a copy of the *Core429_APB Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the Libero online help for instructions on obtaining IP documentation.

For more information about Intellectual Property, visit: <http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>. For updates and additional information about software, FPGAs, and hardware, visit: <http://www.microsemi.com>.

Supported Test Environments

The following test environments are supported:

- Verilog verification testbench
- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

As of Core429_APB v3.11 Legacy Mode is no longer supported.

New Features and Devices

No new features or devices added to this version.

Resolved Issues in the v3.11 Release

Table 1 lists the software action requests (SARs) that were resolved in the Core429_APB v3.11 release.

Table 1. Resolved Issues in the v3.11 Release

SAR No.	Description
62848	User testbench for IGLOO and IGLOOE failing for Obfuscated license

Resolved Issues in the v3.10 Release

Table 2 lists the software action requests (SARs) that were resolved in the Core429_APB v3.10 release.

Table 2. Resolved Issues in the v3.10 Release

SAR No.	Description
40661	A solution has been added to the v3.10 CPZ's.

Resolved Issues in the v3.9 Release

Table 3 lists the SARs that were resolved in the Core429_APB v3.9 release.

Table 3. Resolved Issues in the v3.9 Release

SAR No.	Description
47188	TX_FIFO_FULL flag stays asserted and never de-asserts when data read from tx fifo.

Resolved Issues in the v3.7 Release

Table 4 lists the SARs that were resolved in the Core429_APB v3.7 release.

Table 4. Resolved Issues in the v3.7 Release

SAR No.	Description
39402	Issue with TX_FIFO_FULL generation. This issue was fixed with some additional RTL.

Resolved Issues in the v3.4 Release

Table 5 lists the SARs that were resolved in the Core429_APB v3.4 release.

Table 5. Resolved Issues in the v3.4 Release

SAR No.	Description
38864	Issue in TX_FIFO Flag generation logic. This issue was fixed by modifying the RTL.
38885	Issue in RX FIFO_EMPTY condition. This issue was fixed by modifying the RTL.

Resolved Issues in the v3.1 Release

Table 6 lists the SARs that were resolved in the Core429_APB v3.1 release.

Table 6. Resolved Issues in the v3.1 Release

SAR No.	Description
65765	Added clarification to the description of CLK_FREQ allowed values in the handbook.
65764	The CLK_FREQ parameter from the CoreConsole GUI to the top-level wrapper passed incorrectly. This problem was fixed.
65354	The TX module generates incorrect data rate in VHDL flow. This issue was fixed by modifying the RTL.
65353	The VHDL testbench has a width mismatch for 16-bit and 32-bit data width. This problem was fixed by modifying the testbench.

Resolved Issues in the v3.0 Release

The Core429_APB RTL code used in v3.0 is identical to that in v2.3, apart from the addition of additional FPGA families, and the move to delivery through CoreConsole. There is no need for current customers to upgrade their designs.

Known Limitations and Workarounds

There are no known limitations or workarounds in the Core429_APB v3.11 release.



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