
Core16550 v3.0 Release Notes

This is the production release for the Core16550 IP core. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

Some key features of Core16550 are as follows:

- Transmitter and receiver are each buffered with up to 16-byte FIFOs to reduce the number of interrupts presented to the CPU
- Adds or strips standard asynchronous communication bits (start, stop, and parity)
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator
- Modem control functions (CTS_n, RTS_n, DSR_n, DTR_n, RI_n, and DCD_n)
- Advanced Peripheral Bus (APB) register interface

Delivery Types

Core16550 is licensed in three ways: Evaluation, Obfuscated, and RTL.

Evaluation

Pre-compiled simulation libraries are provided, allowing the core to be instantiated in CoreConsole and simulated within Actel Libero® Integrated Design Environment (IDE). The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with CoreConsole. Simulation, Synthesis, and Layout can be performed with Libero IDE. The RTL code for the core is obfuscated and the some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- Fusion
- IGLOO™/e
- ProASIC®3/E
- ProASIC^{PLUS}®
- Axcelerator®
- RTAX-S

Supported Tool Flows

Use CoreConsole v1.2.1 and Libero IDE v7.3 or later with this Core16550 release.

Install Instructions

The Core16550 CCZ file must be installed using CoreConsole. Using the **Actions > Add to database** function in CoreConsole, locate and install the CCZ file. Then shut down and restart CoreConsole (this should be done when no CoreConsole project is open). Once installed in CoreConsole, the core can be instantiated, configured, and exported to the Libero IDE environment.

For RTL and Obfuscated versions of the core, the FlexLM license must be installed and CoreConsole must be restarted before the core can be exported.

Consult CoreConsole help for further instructions regarding core installation and licensing.

Documentation

The release contains a copy of the *Core16550 Handbook*. The handbook describes the core functionality, gives implementation suggestions, and provides step-by-step instructions on how to simulate, synthesize, and place-and-route this core. The documentation may be viewed by right-clicking in the Core Selection Pane in CoreConsole after the core has been installed.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at <http://www.actel.com>.

Supported Test Environments

The following test environments are supported for Core16550:

- Verilog verification testbench
- VHDL verification testbench

Discontinued Features and Devices

The following features have been discontinued in the v3.0 release:

- Support for the SX-A and RTSX-S family devices
- Support for 16450 and 16750 mode

New Features and Devices

The following new features and devices are included in the v3.0 release:

- Delivery mechanism is now through CoreConsole
- Support of Fusion and IGLOO/e families
- Supports APB interface

Resolved Issues in the v3.0 Release

None.

Known Issues and Workarounds

None.

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