Core1588 v2.0

Handbook

Microsemi

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Introduction

Core1588 Overview

Core1588 provides hardware support for the implementation of an IEEE 1588 Precision Time Protocol (PTP) capable system. A firmware component that interacts with Core1588 will also form part of such a system. Core1588 maintains a Real Time Counter (RTC) and monitors the Ethernet MAC-PHY interface to identify IEEE 1588 type frames. The core timestamps receipt and transmission of these frames and, when enabled, can interrupt the system processor to cause action to be taken. Core1588 supports full duplex operation. An APB interface is present on the core and this allows the system processor to control how the core operates and to retrieve timestamp information.

Latch inputs and trigger outputs are present on Core1588 and these provide the ability to accurately timestamp system events and to effect actions at predefined times. The interrupt mechanism can be used to alert the system processor when a latch or trigger event occurs but the processor does not necessarily have to be critically involved time wise in responding to latch and trigger events. For example, a trigger output could be used directly to cause some other action to occur in the system without waiting for the processor to do something.

Core1588 is currently targeted primarily at SmartFusion devices and it is intended that it will be used in conjunction with the (hard) MAC included within the MSS component of these devices. Core1588 is itself a soft core that will be implemented in the FPGA fabric of a SmartFusion device. The (RMII) MAC-PHY interface of SmartFusion can be made available to the FPGA fabric of the device and this feature is employed to connect Core1588 to the system appropriately, allowing it to monitor Ethernet traffic.

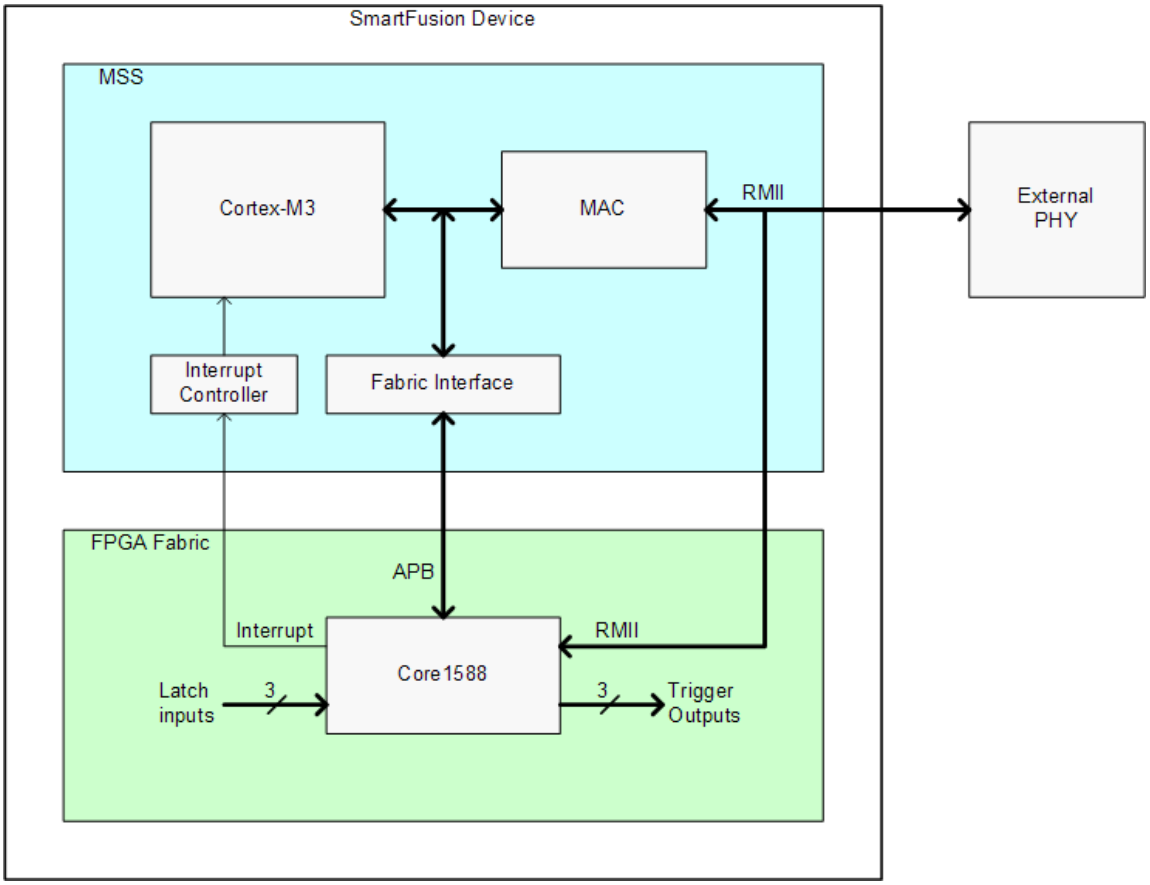

Figure 1 Core1588 in a SmartFusion Device

Key Features

- Real Time Clock (RTC) (32 bit seconds counter and 32 bit nanoseconds counter)
- Supports up to 3 latch inputs and up to 3 trigger outputs
- APB interface for processor access
- RTC value can be written directly
- RTC can be speeded up or slowed down
- Monitors RMII interface to detect IEEE 1588 frames
- Supports full duplex operation
- Can generate interrupt when IEEE 1588 frame detected or when latch/trigger event occurs
- Supports 100 Mbps operation only

Core Version

This handbook supports Core1588 version 2.0.

Supported Device Families

SmartFusion

Supported Interfaces

RMII

Core1588 monitors the RMII interface between a MAC and PHY and detects the transmission and reception of IEEE 1588 frames. The core takes in all the RMII signals as inputs and so does not present a functional RMII interface. Transmit and receive related RMII signals alike are inputs to Core1588.

APB

An APB (version 3) interface is included on the core to allow a system processor to access various control and status registers in the core.

Supported Tool Flows

Core1588 requires Libero v9.1 SP2 or later.

Utilization and Performance

A summary of utilization and performance information for Core1588 is listed in Table 1 through Table 3.

Table 1 Core1588 Device Utilization and Performance (Minimum Configuration)

Family	Tiles			Utilization		Performance (MHz)	
	Sequential	Combinatorial	Total	Device	Total %	PCLK	RMII_CLK
SmartFusion	814	1184	1998	A2F200M3F	44	100	90

Note: Data in this table were achieved using typical synthesis and layout settings. Top level configuration parameters were set to their default values.

Table 2 Core1588 Device Utilization and Performance (Typical Configuration)

Family	Tiles			Utilization		Performance (MHz)	
	Sequential	Combinatorial	Total	Device	Total %	PCLK	RMII_CLK
SmartFusion	948	1436	2384	A2F200M3F	52	100	85

Note: Data in this table were achieved using typical synthesis and layout settings. Top level configuration parameters that differ from their default values were set as follows: TRIG_NUM = 1, LATCH_NUM = 1.

Table 3 Core1588 Device Utilization and Performance (Maximum Configuration)

Family	Tiles			Utilization		Performance (MHz)	
	Sequential	Combinatorial	Total	Device	Total %	PCLK	RMII_CLK
SmartFusion	1217	1974	3191	A2F200M3F	70	100	80

Note: Data in this table were achieved using typical synthesis and layout settings. Top level configuration parameters that differ from their default values were set as follows: TRIG_NUM = 3, LATCH_NUM = 3.

Design Description

Design Implementation

Figure 2 shows an overview of Core1588.

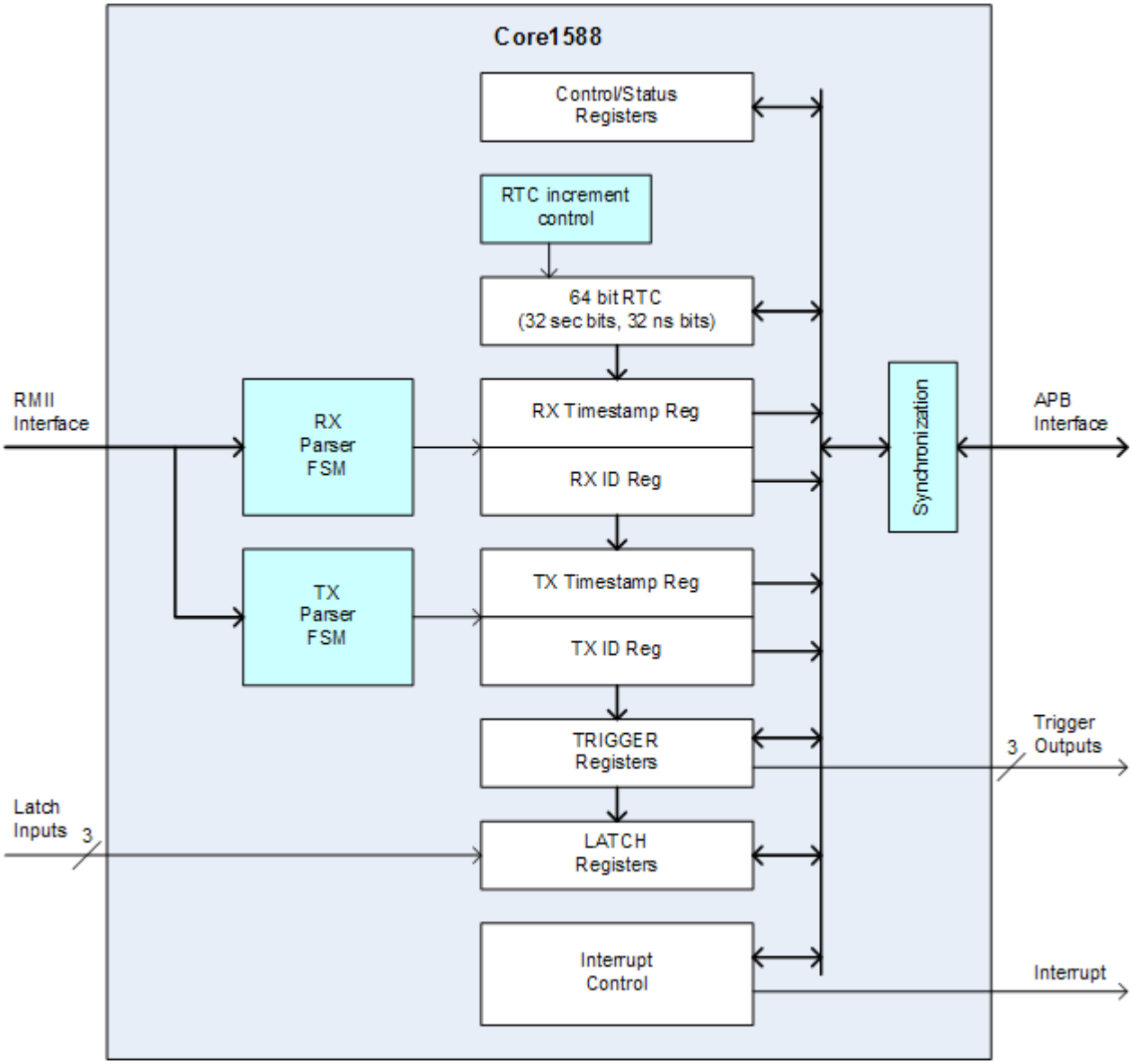

Figure 2 Overview of Core1588

RTC

Core1588 contains an RTC with a 32 bit nanoseconds counter and a 32 bit seconds counter. When the nanoseconds counter reaches 1 x 10^9, it reverts to zero and the seconds counter increments by 1. Through the core's APB interface, the system processor can set the RTC value directly as well as speed up or slow down the RTC rate.

Writing to the RTCL and RTCM registers sets the RTC value. The value written to RTCL is used to update the 32 bit nanoseconds counter and the value written to RTCM updates the 32 bit seconds counter. The RTCL register should be written to first, followed by a write to the RTCM register. The write to RTCL only takes effect when the RTCM register is written to. In this way, all 64 bits of the RTC are updated on the same clock cycle.

When reading the RTC, RTCL should be read first followed by the RTCM register. Reading the RTCL register causes a snapshot to be taken of the 32 bit seconds counter and this snapshot value is returned on the subsequent read of the RTCM. This mechanism ensures that the RTCM and RTCL values are coincident.

The RTC is clocked by the 50 MHz RMII_CLK signal. On each rising edge of RMII_CLK the nanoseconds count increases by 20, when no adjustment is applied. Speeding up or slowing down of the RTC can be achieved by adding more or less than 20 to the count on some rising edges of RMII_CLK. The ADJUST register is used to control adjustment of the RTC. This register contains a five bit adjustment value to add to the nanoseconds count (when not adding the default of 20), an enable bit and 24 bits for a counter rollover value. (The remaining two bits of the 32 bit ADJUST register are reserved.) When the enable bit is set, the 24 bit counter rollover value is used in conjunction with an independent 24 bit counter, also clocked by RMII_CLK. This counter increments by 1 on each RMII_CLK rising edge and when its value matches the 24 bit value held in the ADJUST register the counter returns to zero and begins to increment again. At the same time, the adjustment value held in the upper five bits of the ADJUST register is added to the RTC nanoseconds count instead of the usual value of 20. In this way the nanoseconds count can occasionally be updated by an amount greater than or less than 20, essentially allowing the RTC to be speeded up or slowed down. The amount by which the RTC is sped up or slowed down is a function of how much the adjustment value differs from 20 and how often the adjustment value is used instead of the default of 20. This latter variable is determined by the 24 bit counter rollover value in the ADJUST register. The lower this value, the more often the adjustment value will be used instead of 20. The adjustment value can range from 0 to 31. Figure 3 gives a conceptual overview of how the ADJUST register is used to influence the rate at which the RTC value increases.

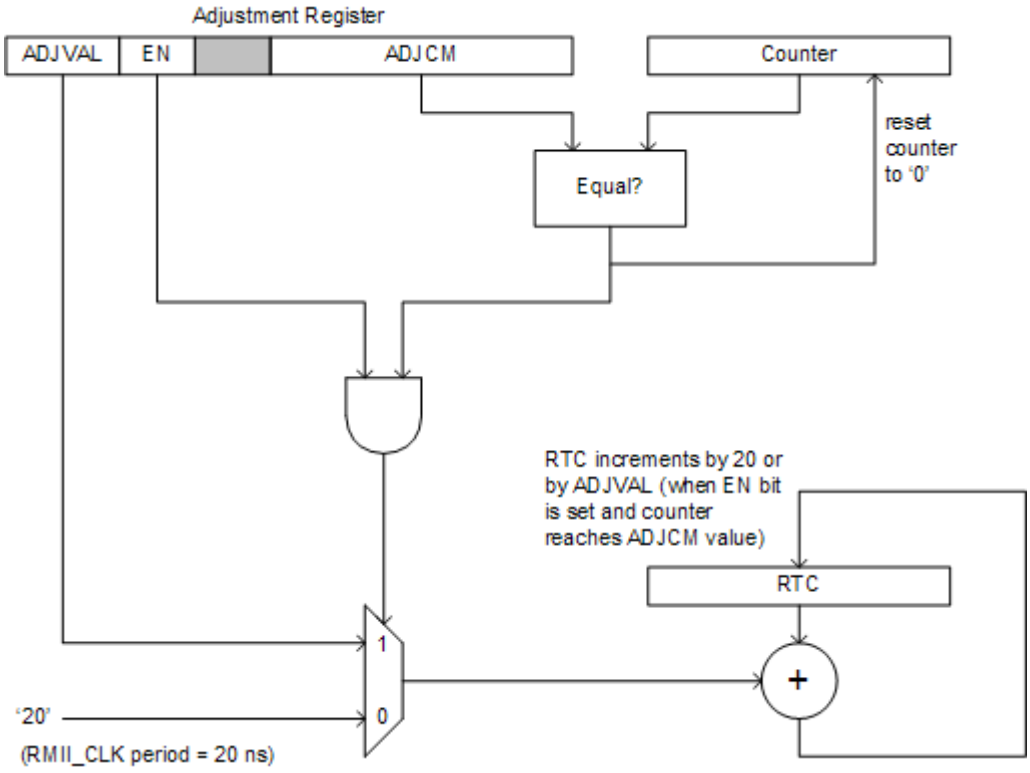

Figure 3 Role of the ADJUST Register in Controlling RTC Rate

Parsing of RMII Traffic

Two finite state machines are used within Core1588 for parsing transmit and receive traffic on the RMII interface. The core supports full duplex operation. When certain IEEE 1588 frames are detected, the core records a timestamp for the relevant frame along with some identification fields from the frame. A timestamp is simply a record of the RTC value at the time when a particular point of the frame traverses the MAC-PHY interface. The timestamp reference point is defined by IEEE 1588 as the beginning of the first symbol after the Start of Frame (SOF) delimiter. Figure 4 illustrates the position of the timestamp reference point in terms of RMII signals.

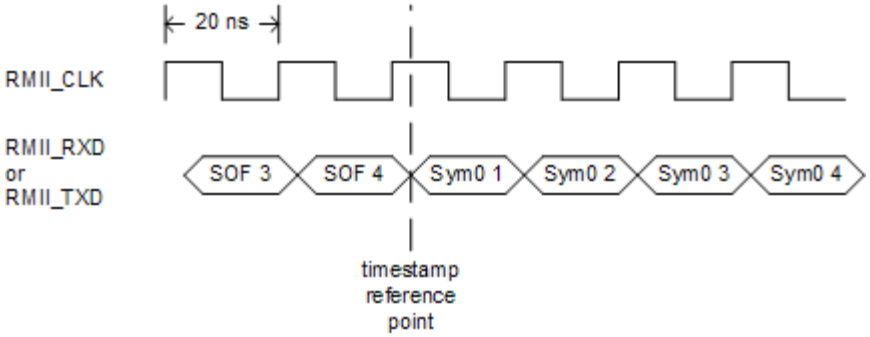

Figure 4 IEEE 15888 Timestamp Reference Point

Frames of Interest

Core1588 only responds to certain IEEE 1588 frames, partly depending on whether it is operating in master or slave mode. The MST_EN bit of the GCFG register determines the mode of operation of the core.

Core1588 only detects transmission of Sync frames when in master mode.

Core1588 only detects transmission of Delay_Req frames when in slave mode.

Transmission of Pdelay_Req and Pdelay_Resp frames is detected regardless of whether the core is operating in master or slave mode.

Reception of Sync, Delay_Req, Pdelay_Req, Pdelay_Resp and Follow_Up frames is always detected in both master and slave mode.

When receipt of a frame of interest is detected the RIRTS bit of the Raw Interrupt Status (RIS) register is set to '1' and when transmission of a frame of interest is detected the RITTS bit of the RIS register is set to '1'. These bits must be cleared by firmware before the receipt/transmission of another frame of interest can be detected and timestamped. It is envisaged that firmware will clear the RIRTS or RITTS bit after reading the relevant timestamp registers. The timestamp registers associated with a received frame are RTSL and RTSM, and the timestamp registers for a transmitted frame are TTSL and TTSM.

Latch Inputs

The core can be configured to support up to three latch inputs. The LATCH_NUM parameter, which can be set using the core's configuration GUI, controls the number of latch inputs supported.

When a rising edge is detected on a latch input, the current RTC value is recorded in latch registers and, if enabled, an interrupt is generated by asserting the INT output. A circuit clocked by the 50 MHz RMII_CLK clock signal is used to detect rising edges on the latch inputs. If the signal driving a latch input is not in the RMII_CLK clock domain then you must ensure that the signal is high for more than one RMII_CLK period, which is equivalent to 20 ns, in order for a rising edge to be detected on the latch input.

The LT0L and LT0M registers are used to record the RTC value when a rising edge is detected on the LATCH0 input. Similarly, the LT1L and LT1M registers are associated with the LATCH1 input and the LT2L and LT2M registers are associated with the LATCH2 input.

There are separate enable bits (LT0_EN, LT1_EN and LT2_EN) in the GCFG register for each of the latch register pairs. If any of these enable bits is set to '0' then the corresponding latch register pair will not be updated when a rising edge is detected on the relevant latch input. The enable bits provide a mechanism to hold a value in a latch register pair even though subsequent rising edges may occur on the relevant latch input. For example, if the LT0_EN bit is '0' then the LT0L and LT0M registers will not be updated when a rising edge occurs on the LATCH0 input.

The IELT0, IELT1 and IELT2 bits of the Interrupt Enable Register (IER) are used to control whether or not rising edges on the latch inputs cause an interrupt to be generated.

Trigger Outputs

Up to three trigger outputs can be provided by the core when it is appropriately configured. The TRIG_NUM parameter, which can be set using the core's configuration GUI, controls the number of trigger outputs supported.

When the RTC reaches a preset trigger value, a pulse is generated on the corresponding trigger output, provided that pulse generation has been enabled for the relevant trigger output. The pulse is a one clock cycle pulse in the RMII_CLK clock domain. The TT0_EN, TT1_EN and TT2_EN bits of the GCFG register control whether or not pulses are generated on the trigger outputs.

An interrupt can also be generated on reaching a trigger time. The IETT0, IETT1 and IETT2 bits of the Interrupt Enable Register (IER) control whether or not an interrupt is generated on a time match.

The TT0L and TT0M registers store the match time for the TRIG0 output. The TT1L and TT1M registers relate to the TRIG1 output, and the TT2L and TT2M registers relate to the TRIG2 output.

Interrupts

Core1588 can interrupt the system processor when various events occur. The Interrupt Enable Register (IER) and the Masked Interrupt Status (MIS) register can be accessed by the system processor to enable or disable interrupts and to identify the source of any pending interrupt. The core can generate an interrupt when a frame of interest is detected on the RMII interface or when a latch or trigger event occurs. See the descriptions for the IER and MIS registers for more details on the bits within these registers.

Interrupts are cleared by writing a '1' to the appropriate bit position or positions in the Raw Interrupt Status (RIS) register.

The RIRTS/RITTS bit of the RIS register will be set on detection of the receipt/transmission of an IEEE 1588 frame of interest. The RIRTS/RITTS bit must be cleared by firmware before receipt/transmission of another frame of interest can be detected and timestamped.

Reset Synchronization

The active low APB reset input (PRESETN) to the core is synchronized to the RMII_CLK clock domain within the core to create a reset signal for logic clocked by RMII_CLK. PRESETN should be asserted (low) for a time exceeding one period of RMII_CLK, which is equivalent to 20ns, to ensure that logic in the RMII_CLK domain is reset successfully.

Register Summary

Table 4 Register Summary

Address Offset	Register Name	Type	Width	Reset Value	Description
0x00	GCFG	R/W	32	0x00000000	General configuration register.
0x04	IER	R/W	32	0x00000000	Interrupt enable register.
0x08	MIS	R	32	0x00000000	Masked interrupt status register.
0x0C	RIS	R/W	32	0x00000000	Raw interrupt status register.
0x10	TTSL	R	32	0x00000000	Transmit timestamp least significant word.
0x14	TTSM	R	32	0x00000000	Transmit timestamp most significant word.
0x18	TTSID	R	32	0x00000000	Transmit timestamp identification register. Contains the 16 bit sequence ID and the 16 port number of the sourcePortIdentity.
0x1C	RTSL	R	32	0x00000000	Receive timestamp least significant word.
0x20	RTSM	R	32	0x00000000	Receive timestamp most significant word.
0x24	RTSID2	R	32	0x00000000	Receive timestamp identification register 2. Contains the 16 bit sequenceId, and the 16 bit port number of the sourcePortIdentity.
0x28	RTSID1	R	32	0x00000000	Receive timestamp identification register 1. Contains bits [63:32] of the sourcePortIdentity.
0x2C	RTSID0	R	32	0x00000000	Receive timestamp identification register 0. Contains bits [31:0] of the sourcePortIdentity.
0x30	RTCL	R/W	32	0x00000000	RTC least significant word. 32 bit nanoseconds count. When writing to the RTC, the RTCL register should always be written first, followed by a write to the RTCM register. When reading the RTC value, the RTCL register should always be read first, followed by a read of the RTCM register.
0x34	RTCM	R/W	32	0x00000000	RTC most significant word. 32 bit seconds count. When writing to the RTC, the RTCL register should always be written first, followed by a write to the RTCM register. When reading the RTC value, the RTCL register should always be read first, followed by a read of the RTCM register.
0x38	ADJUST	R/W	32	0xA0000000	RTC adjustment control register. This control register can be used to adjust the speed of the RTC. See the detailed description of this register for more details.

0x3C	-	-	-	-	Reserved
0x40	TT0L	R/W	32	0x00000000	Time trigger 0 least significant word. When enabled and the TT0L and TT0M registers match the RTC value, a pulse is generated on the TRIG0 output.
0x44	TT0M	R/W	32	0x00000000	Time trigger 0 most significant word. When enabled and the TT0L and TT0M registers match the RTC value, a pulse is generated on the TRIG0 output.
0x48	TT1L	R/W	32	0x00000000	Time trigger 1 least significant word. When enabled and the TT1L and TT1M registers match the RTC value, a pulse is generated on the TRIG1 output.
0x4C	TT1M	R/W	32	0x00000000	Time trigger 1 most significant word. When enabled and the TT1L and TT1M registers match the RTC value, a pulse is generated on the TRIG1 output.
0x50	TT2L	R/W	32	0x00000000	Time trigger 2 least significant word. When enabled and the TT2L and TT2M registers match the RTC value, a pulse is generated on the TRIG2 output.
0x54	TT2M	R/W	32	0x00000000	Time trigger 2 most significant word. When enabled and the TT2L and TT2M registers match the RTC value, a pulse is generated on the TRIG2 output.
0x58	LT0L	R	32	0x00000000	Latch 0 least significant word. When enabled and a rising edge is detected on the LATCH0 input, LT0L stores the LSW of the RTC.
0x5C	LT0M	R	32	0x00000000	Latch 0 most significant word. When enabled and a rising edge is detected on the LATCH0 input, LT0M stores the MSW of the RTC.
0x60	LT1L	R	32	0x00000000	Latch 1 least significant word. When enabled and a rising edge is detected on the LATCH1 input, LT1L stores the LSW of the RTC.
0x64	LT1M	R	32	0x00000000	Latch 1 most significant word. When enabled and a rising edge is detected on the LATCH1 input, LT1M stores the MSW of the RTC.
0x68	LT2L	R	32	0x00000000	Latch 2 least significant word. When enabled and a rising edge is detected on the LATCH2 input, LT2L stores the LSW of the RTC.
0x6C	LT2M	R	32	0x00000000	Latch 2 most significant word. When enabled and a rising edge is detected on the LATCH2 input, LT2M stores the MSW of the RTC.

General Configuration Register

Table 5 General Configuration Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x00	GCFG	R/W	32	0x00000000	General core configuration register.

Table 6 General Configuration Register Bit Definitions

Bits	Name	Type	Description
31:16			Reserved
15	LT2_EN	R/W	0: Disable latch 2 timestamp registers 1: Enable latch 2 timestamp registers This bit must be set to '1' in order for the LT2L and LT2M registers to be updated with the RTC value when a rising edge is observed on the LATCH2 input.
14	LT1_EN	R/W	0: Disable latch 1 timestamp registers 1: Enable latch 1 timestamp registers This bit must be set to '1' in order for the LT1L and LT1M registers to be updated with the RTC value when a rising edge is observed on the LATCH1 input.
13	LT0_EN	R/W	0: Disable latch 0 timestamp registers 1: Enable latch 0 timestamp registers This bit must be set to '1' in order for the LT0L and LT0M registers to be updated with the RTC value when a rising edge is observed on the LATCH0 input.
12	TT2_EN	R/W	0: Disable TRIG2 output 1: Enable TRIG2 output This bit must be set to '1' in order for a pulse to be generated on the TRIG2 output when the RTC value reaches the time set in the TT2L and TT2M registers.
11	TT1_EN	R/W	0: Disable TRIG1 output 1: Enable TRIG1 output This bit must be set to '1' in order for a pulse to be generated on the TRIG1 output when the RTC value reaches the time set in the TT1L and TT1M registers.
10	TT0_EN	R/W	0: Disable TRIG0 output 1: Enable TRIG0 output This bit must be set to '1' in order for a pulse to be generated on the TRIG0 output when the RTC value reaches the time set in the TT0L and TT0M registers.
9:4			Reserved
3	MST_EN	R/W	0: Core is operating in slave mode 1: Core is operating in master mode
2:1			Reserved
0	ENCOR	R/W	0: Disable core 1: Enable core

Interrupt Enable Register

Table 7 Interrupt Enable Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x04	IER	R/W	32	0x00000000	Interrupt enable register

Table 8 Interrupt Enable Register Bit Definitions

Bits	Name	Type	Description
31:8			Reserved
7	IELT2	R/W	0: Disable latch 2 interrupt (ILT2) 1: Enable latch 2 interrupt (ILT2)
6	IELT1	R/W	0: Disable latch 1 interrupt (ILT1) 1: Enable latch 1 interrupt (ILT1)
5	IELT0	R/W	0: Disable latch 0 interrupt (ILT0) 1: Enable latch 0 interrupt (ILT0)
4	IETT2	R/W	0: Disable trigger 2 interrupt (ITT2) 1: Enable trigger 2 interrupt (ITT2)
3	IETT1	R/W	0: Disable trigger 1 interrupt (ITT1) 1: Enable trigger 1 interrupt (ITT1)
2	IETT0	R/W	0: Disable trigger 0 interrupt (ITT0) 1: Enable trigger 0 interrupt (ITT0)
1	IERTS	R/W	0: Disable receive timestamp interrupt (IRTS) 1: Enable receive timestamp interrupt (IRTS)
0	IETTS	R/W	0: Disable transmit timestamp interrupt (ITTS) 1: Enable transmit timestamp interrupt (ITTS)

Masked Interrupt Status Register

Table 9 Masked Interrupt Status Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x08	MIS	R	32	0x00000000	Masked interrupt status register

Table 10 Masked Interrupt Status Register Bit Definitons

Bits	Name	Type	Description
31:8			Reserved
7	ILT2	R	This bit is the logical AND of bit 7 of IER and bit 7 of RIS
6	ILT1	R	This bit is the logical AND of bit 6 of IER and bit 6 of RIS
5	ILT0	R	This bit is the logical AND of bit 5 of IER and bit 5 of RIS
4	ITT2	R	This bit is the logical AND of bit 4 of IER and bit 4 of RIS
3	ITT1	R	This bit is the logical AND of bit 3 of IER and bit 3 of RIS
2	ITT0	R	This bit is the logical AND of bit 2 of IER and bit 2 of RIS
1	IRTS	R	This bit is the logical AND of bit 1 of IER and bit 1 of RIS
0	ITTS	R	This bit is the logical AND of bit 0 of IER and bit 0 of RIS

Note: All the bits of the Masked Interrupt Status register are ORed together to generate the INT output from the core.

Raw Interrupt Status Register

Table 11 Raw Interrupt Status Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x0C	RIS	R/W	32	0x00000000	Raw Input Status Register

Table 12 Raw Interrupt Status Register Bit Definitions

Bits	Name	Type	Description
31:8			Reserved
7	RILT2	R/W	When this bit has a value of '1' it indicates that a rising edge has been observed on the LATCH2 input since this bit was last '0'. This bit is cleared by writing '1' to it. Writing '0' has no effect.
6	RILT1	R/W	When this bit has a value of '1' it indicates that a rising edge has been observed on the LATCH1 input since this bit was last '0'. This bit is cleared by writing '1' to it. Writing '0' has no effect.
5	RILT0	R/W	When this bit has a value of '1' it indicates that a rising edge has been observed on the LATCH0 input since this bit was last '0'. This bit is cleared by writing '1' to it. Writing '0' has no effect.
4	RITT2	R/W	When this bit has a value of '1' it indicates that the time set in the trigger 2 registers (TT2L and TT2M) has been reached since this bit was last '0'. This bit is cleared by writing '1' to it. Writing '0' has no effect.
3	RITT1	R/W	When this bit has a value of '1' it indicates that the time set in the trigger 1 registers (TT1L and TT1M) has been reached since this bit was last '0'. This bit is cleared by writing '1' to it. Writing '0' has no effect.
2	RITT0	R/W	When this bit has a value of '1' it indicates that the time set in the trigger 0 registers (TT0L and TT0M) has been reached since this bit was last '0'. This bit is cleared by writing '1' to it. Writing '0' has no effect.
1	RIRTS	R/W	When this bit has a value of '1' it indicates that, since this bit was last '0', receipt of an IEEE 1588 frame has been detected and that the receive timestamp registers (RTSL and RTSM) have been updated. This bit is cleared by writing '1' to it. Writing '0' has no effect.
Note: After this bit has been set to '1' by the frame detection hardware, it must be cleared by firmware before receipt of another frame can be detected. It is envisaged that firmware will clear this bit after reading the RTSL and RTSM registers.			
0	RITTS	R/W	When this bit has a value of '1' it indicates that, since this bit was last '0', transmission of an IEEE 1588 frame has been detected and that the transmit timestamp registers (TTSL and TTSM) have been updated. This bit is cleared by writing '1' to it. Writing '0' has no effect.
Note: After this bit has been set to '1' by the frame detection hardware, it must be cleared by firmware before transmission of another frame can be detected. It is envisaged that firmware will clear this bit after reading the TTSL and TTSM registers.			

Transit Timestamp Least Significant Word Register

Table 13 Transit Timestamp LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x10	TTSL	R	32	0x00000000	Transit timestamp least significant word

Transit Timestamp Most Significant Word Register

Table 14 Transit Timestamp MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x14	TTSM	R	32	0x00000000	Transit timestamp most significant word

Transit Timestamp Identification Register

Table 15 Transit Timestamp Identification Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x18	TTSID	R	32	0x00000000	Transit timestamp identification register. Contains the 16 bit sequence ID and the 16 port number of the sourcePortIdentity.

Table 16 Transit Timestamp Identification Register Bit Definitions

Bits	Name	Type	Description
31:16	TTSSID	R	Stores the sequenceID from the message header of the frame associated with the current transit timestamp (in the TTSL and TTSM registers)
15:0	TTSPN	R	Stores the port number from the message header of the frame associated with the current transmit timestamp (in the TTSL and TTSM registers). (The port number is part of the sourcePortIdentity field of the IEEE 1588 message header.)

Receive Timestamp Least Significant Word Register

Table 17 Receive Timestamp LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x1C	RTSL	R	32	0x00000000	Receive timestamp least significant word

Receive Timestamp Most Significant Word Register

Table 18 Receive Timestamp MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x20	RTSM	R	32	0x00000000	Receive timestamp most significant word

Receive Timestamp Identification Register 2

Table 19 Receive Timestamp Identification Register 2 Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x24	RTSID2	R	32	0x00000000	Receive timestamp identification register 2. Contains the 16 bit sequenceId and the 16 bit port number of the sourcePortIdentity.

Table 20 Receive Timestamp Identification Register 2 Bit Definitions

Bits	Name	Type	Description
31:16	RTSSID	R	Stores the sequenceID from the message header of the frame associated with the current receive timestamp (in the RTSL and RTSM registers).
15:0	RTSPN	R	Stores the port number from the message header of the frame associated with the current receive timestamp (in the RTSL and RTSM registers). (The port number is part of the sourcePortIdentity field of the IEEE 1588 message header.)

Receive Timestamp Identification Register 1

Table 21 Receive Timestamp Identification Register 1 Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x28	RTSID1	R	32	0x00000000	Receive timestamp identification register 1. Contains bits [63:32] of the sourcePortIdentity.

Receive Timestamp Identification Register 0

Table 22 Receive Timestamp Identification Register 0 Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x2C	RTSID0	R	32	0x00000000	Receive timestamp identification register 0. Contains bits [31:0] of the sourcePortIdentity.

RTC Least Significant Word Register

Table 23 RTC LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x30	RTCL	R/W	32	0x00000000	RTC least significant word. 32 bit nanoseconds count. When writing to the RTC, the RTCL register should always be written first, followed by a write to the RTCM register. When reading the RTC value, the RTCL register should always be read first, followed by a read of the RTCM register.

RTC Most Significant Word Register

Table 24 RTC MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x34	RTCM	R/W	32	0x00000000	RTC most significant word. 32 bit seconds count. When writing to the RTC, the RTCL register should always be written first, followed by a write to the RTCM register. When reading the RTC value, the RTCL register should always be read first, followed by a read of the RTCM register.

Adjustment Register

Table 25 Adjustment Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x38	ADJUST	R/W	32	0xA0000000	This control register can be used to adjust the speed of the RTC. See the detailed description of this register for more details.

Table 26 Adjustment Register Bit Definitions

Bits	Name	Type	Description
31:27	ADJVAL	R/W	This five bit field holds the amount to be added to RTC least significant word (nanoseconds count) each time the adjustment counter returns to zero (and the ADJEN bit is set to 1). The RTC operates in the 50 MHz RMII_CLK clock domain and the nanoseconds count normally increments by 20 on each rising edge of RMII_CLK. When the conditions described above are met, the RTC will be incremented by the value stored in ADJVAL, instead of by the normal amount of 20. The value stored in ADJVAL can range from 0 to 31. Using adjustment with an ADJVAL value less than 20 will result in a slowing down of the RTC. Similarly, using adjustment with an ADJVAL greater than 20 will cause the RTC to speed up. The amount of slowing down or speeding up is a function of both the ADJVAL value and the ADJCM value.
26	ADJEN	R/W	0: Adjustment feature is disabled 1: Adjustment feature is enabled
25:24	-	-	Reserved
23:0	ADJCM	R/W	Adjustment counter maximum value. This field sets the rollover value for a 24 bit adjustment counter clocked by RMII_CLK. The adjustment counter is essentially a free running counter that increments by 1 on each rising edge of RMII_CLK. When the counter value reaches the ADJCM value it returns to zero and, if the ADJEN bit is set, the RTC nanoseconds count is incremented by the ADJVAL instead of by the normal amount of 20. The ADJCM field essentially controls how frequently the ADJVAL is used as the RTC increment.

Time Trigger 0 Least Significant Word Register

Table 27 Time Trigger 0 LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x40	TT0L	R/W	32	0x00000000	Time trigger 0 least significant word. This register is only relevant if the core has been configured to support 1 or more trigger outputs (TRIG_NUM parameter set to 1 or greater). When the RTC value (RTCL & RTCM) reaches the time set in the TT0L and TT0M registers, the RITT0 bit of the RIS register will be set to '1' (or will remain at '1' if it is already '1'). An interrupt can be generated on the time match (depending on the value of the IETT0 bit of the IER) and/or a pulse can be generated on the TRIG0 output (depending on the value of the TT0_EN bit of the GCFG register).

Time Trigger 0 Most Significant Word Register

Table 28 Time Trigger 0 MSW Register Definition

Address Offset	Register Name	Type	Width	Reset Value	Description
0x44	TT0M	R/W	32	0x00000000	Time trigger 0 most significant word. This register is only relevant if the core has been configured to support 1 or more trigger outputs (TRIG_NUM parameter set to 1 or greater). When the RTC value (RTCL & RTCM) reaches the time set in the TT0L and TT0M registers, the RITT0 bit of the RIS register will be set to '1' (or will remain at '1' if it is already '1'). An interrupt can be generated on the time match (depending on the value of the IETT0 bit of the IER) and/or a pulse can be generated on the TRIG0 output (depending on the value of the TT0_EN bit of the GCFG register).

Time Trigger 1 Least Significant Word Register

Table 29 Time Trigger 1 LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x48	TT1L	R/W	32	0x00000000	Time trigger 1 least significant word. This register is only relevant if the core has been configured to support 2 or more trigger outputs (TRIG_NUM parameter set to 2 or greater). When the RTC value (RTCL & RTCM) reaches the time set in the TT1L and TT1M registers, the RITT1 bit of the RIS register will be set to '1' (or will remain at '1' if it is already '1'). An interrupt can be generated on the time match (depending on the value of the IETT1 bit of the IER) and/or a pulse can be generated on the TRIG1 output (depending on the value of the TT1_EN bit of the GCFG register).

Time Trigger 1 Most Significant Word Register

Table 30 Time Trigger 1 MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x4C	TT1M	R/W	32	0x00000000	Time trigger 1 most significant word. This register is only relevant if the core has been configured to support 2 or more trigger outputs (TRIG_NUM parameter set to 2 or greater). When the RTC value (RTCL & RTCM) reaches the time set in the TT1L and TT1M registers, the RITT1 bit of the RIS register will be set to '1' (or will remain at '1' if it is already '1'). An interrupt can be generated on the time match (depending on the value of the IETT1 bit of the IER) and/or a pulse can be generated on the TRIG1 output (depending on the value of the TT1_EN bit of the GCFG register).

Time Trigger 2 Least Significant Word Register

Table 31 Time Trigger 2 LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x50	TT2L	R/W	32	0x00000000	Time trigger 2 least significant word. This register is only relevant if the core has been configured to support 3 trigger outputs (TRIG_NUM parameter set to 3). When the RTC value (RTCL & RTCM) reaches the time set in the TT2L and TT2M registers, the RITT2 bit of the RIS register will be set to '1' (or will remain at '1' if it is already '1'). An interrupt can be generated on the time match (depending on the value of the IETT2 bit of the IER) and/or a pulse can be generated on the TRIG2 output (depending on the value of the TT2_EN bit of the GCFG register).

Time Trigger 2 Most Significant Word Register

Table 32 Time Trigger 2 MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x54	TT2M	R/W	32	0x00000000	Time trigger 2 most significant word. This register is only relevant if the core has been configured to support 3 trigger outputs (TRIG_NUM parameter set to 3). When the RTC value (RTCL & RTCM) reaches the time set in the TT2L and TT2M registers, the RITT2 bit of the RIS register will be set to '1' (or will remain at '1' if it is already '1'). An interrupt can be generated on the time match (depending on the value of the IETT2 bit of the IER) and/or a pulse can be generated on the TRIG2 output (depending on the value of the TT2_EN bit of the GCFG register).

Latch 0 Least Significant Word Register

Table 33 Latch 0 LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x58	LT0L	R	32	0x00000000	Latch 0 least significant word. This register is only relevant if the core has been configured to support 1 or more latch inputs (LATCH_NUM parameter set to 1 or greater). When a rising edge is detected on the LATCH0 input, the value in the RTCL register will be stored in this register if the LT0_EN bit of the GCFG register is set to '1'. This register will hold its current value if the LT0_EN bit of the GCFG register is '0'. The detection of a rising edge on the LATCH0 input will also cause the RILT0 bit of the RIS register to be set to '1' (if it is not already set to '1'). This can in turn cause assertion of the INT interrupt output if the IELT0 bit of the IER is set to '1'.

Latch 0 Most Significant Word Register

Table 34 Latch 0 MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x5C	LT0M	R	32	0x00000000	Latch 0 most significant word. This register is only relevant if the core has been configured to support 1 or more latch inputs (LATCH_NUM parameter set to 1 or greater). When a rising edge is detected on the LATCH0 input, the value in the RTCM register will be stored in this register if the LT0_EN bit of the GCFG register is set to '1'. This register will hold its current value if the LT0_EN bit of the GCFG register is '0'. The detection of a rising edge on the LATCH0 input will also cause the RILT0 bit of the RIS register to be set to '1' (if it is not already set to '1'). This can in turn cause assertion of the INT interrupt output if the IELT0 bit of the IER is set to '1'.

Latch 1 Least Significant Word Register

Table 35 Latch 1 LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x60	LT1L	R	32	0x00000000	Latch 1 least significant word. This register is only relevant if the core has been configured to support 2 or more latch inputs (LATCH_NUM parameter set to 2 or greater). When a rising edge is detected on the LATCH1 input, the value in the RTCL register will be stored in this register if the LT1_EN bit of the GCFG register is set to '1'. This register will hold its current value if the LT1_EN bit of the GCFG register is '0'. The detection of a rising edge on the LATCH1 input will also cause the RILT1 bit of the RIS register to be set to '1' (if it is not already set to '1'). This can in turn cause assertion of the INT interrupt output if the IELT0 bit of the IER is set to '1'.

Latch 1 Most Significant Word Register

Table 36 Latch 1 MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x64	LT1M	R	32	0x00000000	Latch 1 most significant word. This register is only relevant if the core has been configured to support 2 or more latch inputs (LATCH_NUM parameter set to 2 or greater). When a rising edge is detected on the LATCH1 input, the value in the RTCM register will be stored in this register if the LT1_EN bit of the GCFG register is set to '1'. This register will hold its current value if the LT1_EN bit of the GCFG register is '0'. The detection of a rising edge on the LATCH1 input will also cause the RILT1 bit of the RIS register to be set to '1' (if it is not already set to '1'). This can in turn cause assertion of the INT interrupt output if the IELT1 bit of the IER is set to '1'.

Latch 2 Least Significant Word Register

Table 37 Latch 2 LSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x68	LT2L	R	32	0x00000000	Latch 2 least significant word. This register is only relevant if the core has been configured to support 3 latch inputs (LATCH_NUM parameter set to 3). When a rising edge is detected on the LATCH2 input, the value in the RTCL register will be stored in this register if the LT2_EN bit of the GCFG register is set to '1'. This register will hold its current value if the LT2_EN bit of the GCFG register is '0'. The detection of a rising edge on the LATCH2 input will also cause the RILT2 bit of the RIS register to be set to '1' (if it is not already set to '1'). This can in turn cause assertion of the INT interrupt output if the IELT2 bit of the IER is set to '1'.

Latch 2 Most Significant Word Register

Table 38 Latch 2 MSW Register Description

Address Offset	Register Name	Type	Width	Reset Value	Description
0x6C	LT2M	R	32	0x00000000	Latch 2 most significant word. This register is only relevant if the core has been configured to support 3 latch inputs (LATCH_NUM parameter set to 3). When a rising edge is detected on the LATCH2 input, the value in the RTCM register will be stored in this register if the LT2_EN bit of the GCFG register is set to '1'. This register will hold its current value if the LT2_EN bit of the GCFG register is '0'. The detection of a rising edge on the LATCH2 input will also cause the RILT2 bit of the RIS register to be set to '1' (if it is not already set to '1'). This can in turn cause assertion of the INT interrupt output if the IELT2 bit of the IER is set to '1'.

Parameters

Table 39 Core1588 Parameter Descriptions

Parameter Name	Valid Range	Default Value	Description
TRIG_NUM	0 to 3	0	Number of trigger outputs
LATCH_NUM	0 to 3	0	Number of latch inputs

Ports

Table 40 Core1588 Port Descriptions

Parameter Name	Valid Range	Default Value
PCLK	In	APB clock
PRESETN	In	APB reset
PADDR[6:0]	In	APB address
PSEL	In	APB select
PENABLE	In	APB enable
PWRITE	In	APB write
PWDATA[31:0]	In	APB write data
PRDATA[31:0]	Out	APB read data
PREADY	Out	APB ready
PSLVERR	Out	APB slave error
INT	Out	Interrupt signal
RMII_CLK	In	RMII clock
RMII_CRSDV	In	RMII carrier sense/data valid
RMII_RXD[1:0]	In	RMII receive data
RMII_RXER	In	RMII receive error
RMII_TXD[1:0]	In	RMII transmit data
RMII_TXEN	In	RMII transmit enable
TRIG0	Out	Trigger 0 A one clock cycle pulse (in the RMII_CLK clock domain) is generated on this output when the internal RTC value reaches the value preset in the TT0L and TT0M registers.
TRIG1	Out	Trigger 1 A one clock cycle pulse (in the RMII_CLK clock domain) is generated on this output when the internal RTC value reaches the value preset in the TT1L and TT1M registers.
TRIG2	Out	Trigger 2 A one clock cycle pulse (in the RMII_CLK clock domain) is generated on this output when the internal RTC value reaches the value preset in the TT2L and TT2M registers.

LATCH0	In	Latch 0 When a rising edge is detected on this input, the current RTC value is latched into the LT0L and LT0M registers.
LATCH1	In	Latch 1 When a rising edge is detected on this input, the current RTC value is latched into the LT1L and LT1M registers.
LATCH2	In	Latch 2 When a rising edge is detected on this input, the current RTC value is latched into the LT2L and LT2M registers.

Licensing

Core1588 is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated, configured, and generated within SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero Integrated Design Environment (IDE). The RTL code for the core is obfuscated.

RTL

Complete RTL source code is provided for the core.

SmartDesign

Core1588 is available for download to the SmartDesign IP Catalog via the Libero IDE web repository. For information on using SmartDesign to instantiate, configure, connect, and generate cores, refer to the Libero IDE online help.

Figure 5 shows an example of an instantiated view of Core1588 on the SmartDesign canvas. The core can be configured using its configuration GUI, as shown in Figure 6.

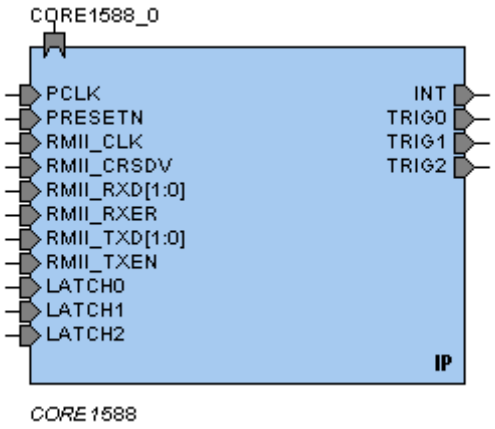

Figure 5 Example Instantiation of Core1588 on SmartDesign Canvas

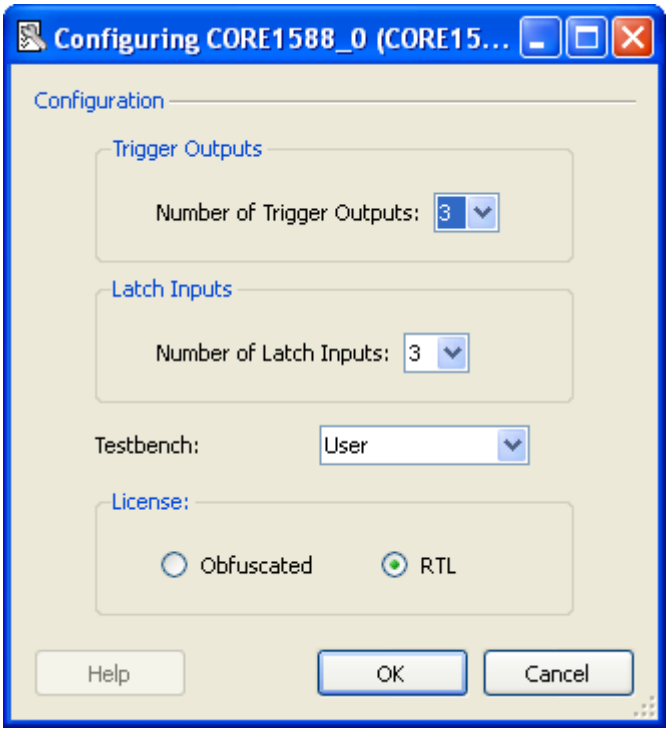

Figure 6 Core1588 Configuration GUI

Simulation Flow

SmartDesign and Libero IDE facilitate running a user testbench for Core1588. To run the user testbench, set the Testbench configuration option to User in the Core1588 configuration GUI before generating the design. After generation, set the design root to be the Core1588 instance and click the Simulation (ModelSim) button. ModelSim will launch and run the unit test.

Synthesis in Libero IDE

To run synthesis with the configuration selected in the configuration GUI, set the design root appropriately and click the Synthesis icon in Libero IDE to launch the Synplicity synthesis tool. Click the Run button in the synthesis window to run synthesis.

Place and Route in Libero IDE

Having set the design root appropriately and run Synthesis, click the Place&Route icon in Libero IDE to invoke Designer.

Connecting Core1588 in SmartDesign

This chapter provides various hints to ease the process of implementation and integration of Core1588 into your design.

Figure 7 shows a SmartDesign design that illustrates the connections required between Core1588 and the SmartFusion MSS. The MSS component has been configured to provide the RMII_CLK clock signal (via its GLC output) which connects both to Core1588 and to the top level of the design so that it can drive the external PHY. The MSS has also been configured to provide clock and reset signals to drive the PCLK and PRESETN inputs of Core1588 and to provide an interrupt input (FABINT) to accept the interrupt signal from Core1588. The MSS has been configured to make the RMII MAC-PHY interface available to the fabric and these signals, named MAC_0_CAPTURE_* on the MSS component, connect to the RMII_* inputs of Core1588. Finally, the MSS has been configured to provide an APB master interface to the fabric and this connects to Core1588's APB interface through the CoreAPB3 bus component.

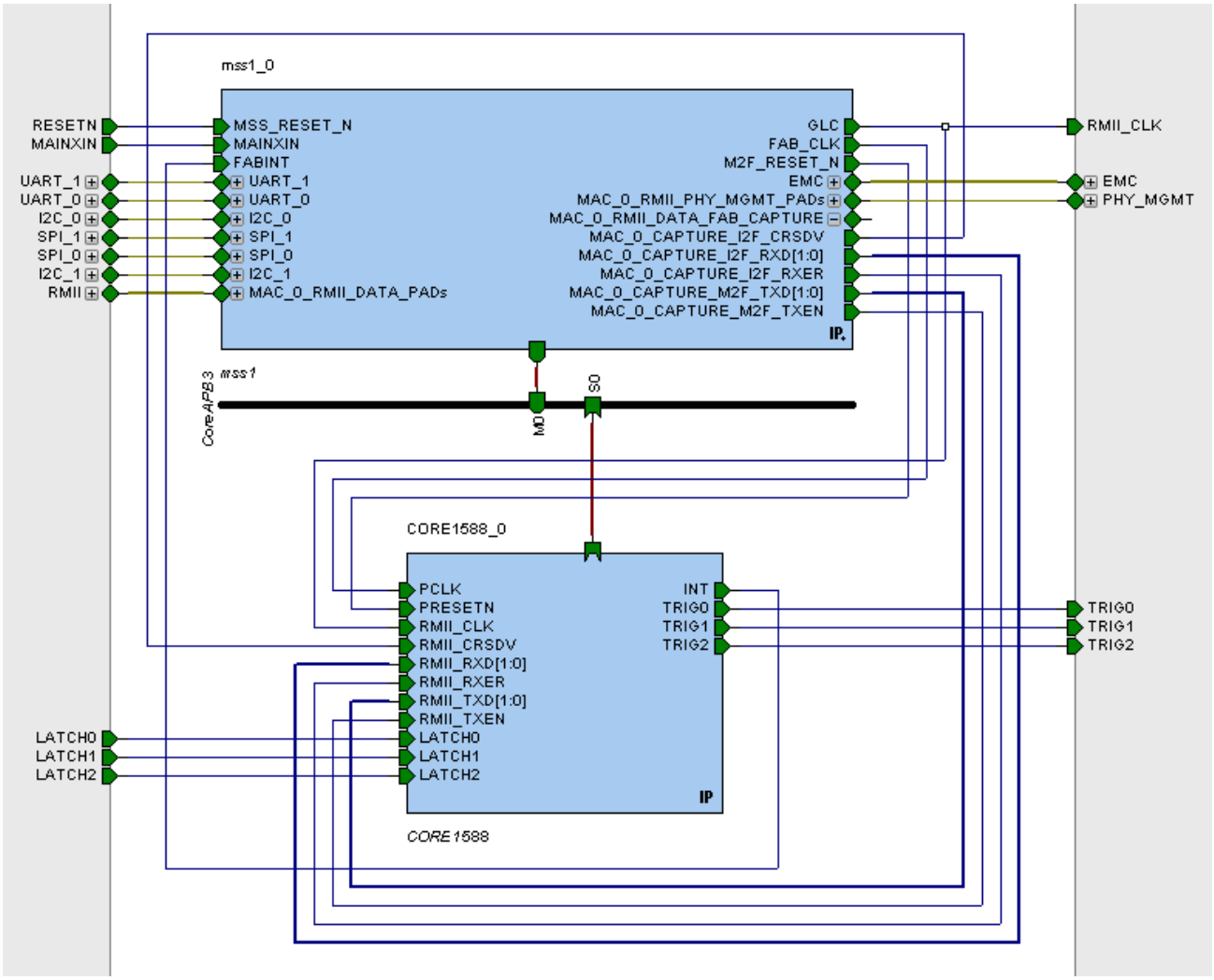

Figure 7 Core1588 System Example

Ordering Information

Ordering Codes

Core1588 can be ordered through your local Sales Representative. It should be ordered using the following number scheme: Core1588-XX, where XX is listed in Table 41.

Table 41 Ordering Codes

XX	Description
OM	RTL for Obfuscated RTL—multiple use license
RM	RTL for RTL source — multiple-use license

Product Support

Microsemi backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group (formerly Actel) and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

Customer Technical Support Center

Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (http://www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at http://www.actel.com/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

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