
Core1553BRT_APB v3.2 Release Notes

This is the first production release for the Core1553BRT_APB IP core. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

- APB3 compliant host interface
- MIL-STD-1553B compliant Remote Terminal
- Supports 12, 16, 20 and 24 MHz operation.
- Fail-safe state machines
- Base core 1553BRT function
- Tested according to RT Validation Test Plan MIL-HDBK-1553, Appendix A

Interfaces

The Core1553BRT_APB core supports an APB3 compliant host interface

Delivery Types

The Core1553BRT_APB core is licensed in three ways: Evaluation, Obfuscated, and RTL.

Evaluation

Precompiled simulation libraries are provided, allowing the core to be instantiated and simulate within Actel Libero[®] Integrated Design Environment (IDE). The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign.

Simulation, Synthesis, and Layout can be performed with Libero IDE. The RTL code for the core is obfuscated and the some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- SmartFusion™
- Fusion
- ProASIC^{PLUS}®
- Axcelerator®
- RTAX-S

Supported Tool Flows

Use Libero IDE v9.0 or later with this Core1553BRT_APB release.

Installation Instructions

Within Libero IDE, click the **Add Core** button in the catalog to locate and install a local CCZ file, or use the automatic web update feature in Libero IDE. Once the CCZ file is installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project. If a license is required, install it in the Libero IDE license file. Refer to the Libero IDE online help for instructions about core installation and licensing.

Documentation

This release contains a copy of the *Core1553BRT_APB Handbook*, which describes the core functionality, gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions.

For updates and additional information about the software, devices, hardware, and documentation, visit the Intellectual Property pages on the Actel website at <http://www.actel.com>.

Supported Test Environments

The following test environments are supported:

- VHDL verification testbench
- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

No features have been discontinued in this release.

Core Versions

The built-in test register (BIT) indicates the version of the core. The core will transmit this in response to the Transmit BIT mode code. [Table 1](#) shows how the versions are encoded.

Table 1 • Encoding of Version Number

Version	BitWord[4:0]
v3.2	10

Release History

[Table 2](#) provides the release history of the core.

Table 2 • Release History

Version	Date
v3.2	June 2010

This document reflects the release and revision history for Core155BRT_APB. The associated release notes for Core1553BRT contain a full release and revision history for the base 1553B function of this core.

Known Issues and Workarounds

There are no known issues in the current release.



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