
Core10100 Core10100_AHBAPB v4.0 Release Notes

This is the production release for the Core10100 and Core10100_AHBAPB IP cores. These release notes describe the features and enhancements. They also contain information about system requirements, supported families, implementations, and known issues and workarounds.

Features

The Core10100 core supports the following:

- Ethernet media access controller
- IEEE 802.3a CSMA/CD
- AHB master and APB slave interfaces or synchronous interface
- 8-, 16-, and 32-bit host interface
- RMI or MII PHY interface

Interfaces

Core10100 is available with two interface types:

- Core10100: Legacy interface with simple synchronous register and memory interfaces
- Core10100_AHBAPB: AMBA AHB master memory interface and AMBA APB register interfaces

Delivery Types

Core10100 is licensed in two ways: Obfuscated and RTL.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Actel Libero[®] Integrated Design Environment (IDE). The RTL code for the core is obfuscated, and some of the testbench source files are not provided. They are precompiled into the compiled simulation library instead.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- IGLOO®
- IGLOOe
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Fusion
- ProASIC^{PLUS}®
- Axcelerator®
- RTAX-S

Supported Tool Flows

Use Libero IDE v8.5 or later with this Core10100 release.

Installation Instructions

The Core10100 CCZ file must be installed into Libero IDE. This is done automatically via the Catalog update function in Libero IDE, or the CCZ file can be manually added using the Add Core catalog feature.

Once installed in the Libero IDE Catalog, the core can be instantiated and configured. If a license is required, it must be installed in the Libero IDE license file.

Consult Libero IDE help for further instructions on core installation, licensing, and general use.

Documentation

The release contains a copy of the *Core10100 Handbook*. The handbook describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, as well as implementation suggestions (see “Known Issues and Workarounds” on page 6).

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Actel website at <http://www.actel.com>.

Supported Test Environments

The following test environments are supported.

Core10100

VHDL User testbench

Verilog User testbench

Core10100_AHBAPB

VHDL User testbench

Verilog User testbench

Discontinued Features and Devices

No features have been discontinued in the v4.0 Core10100 release.

New Features and Devices

The RMI interface was added. ProASIC3L family devices have been added in the v4.0 Core10100 release.

Release History

Table 1 details the release history of this core.

Table 1 · Core10100 Release History

Core Version	Date	Changes
4.0	21 Jan 09	Core name changed to Core10100 from Core10/100. Added RMI interface Fixed SARS listed in Table 2 on page 4 Delivery mechanism through SmartDesign
3.3	3 Mar 08	Fixed SARS listed in Table 3 on page 43
3.2	3 Jan 08	Fixed SARS listed in Table 4 on page 5
3.1	16 Nov 07	Support of IGLOO/e families Fixed SARS listed in Table 5 on page 5
3.0	24 Sep 07	Delivery mechanism through CoreConsole Support of AHB/APB interfaces Support of Fusion family Fixed SARS listed in Table 6 on page 6

Resolved Issues in the v4.0 Release

Table 2 lists the Software Action Requests (SARs) that were resolved in the Core10100 v4.0 release.

Table 2 · Resolved Issues in the v4.0 Release

SAR	Description
78913	HBURST value tied to 0 even if core supports bursts. When HBURST is tied to 0, the core supports single transfers only. Modified the value of HBURST to support burst transfers.
78923	Delta delay issue in clocks between Transmit RAM and MAC. Two clocks are used for transmit RAM and MAC which have skew between them. Modified to single clock to avoid clock skew.
78926	Delta delay issue between clocks of ADDRESS FILTER RAM and MAC. Two clocks are used for ADDRESS FILTER RAM and MAC which have skew between them. Modified to single clock to avoid clock skew.
78967	CSR0 value not updated to reset value after soft reset. Updated the RTL to fix the issue.
78971	CSR11 [15:0] does not get updated for jumbled address 8-bit access. The CSR11[16] CON bit should always be written before the timer value is written. The handbook was updated.
11757	The handbook incorrectly explains how the hash mode address filtering operates; in particular, how to calculate the hash values. The handbook was updated.
12303	TX Data corrupts due to FIFO full when AHB_DWIDTH = 16. The issue was fixed by updating the RTL.

Resolved Issues in the v3.3 Release

Table 3 lists the Software Action Requests (SARs) that were resolved in the Core10100 v3.3 release.

Table 3 · Resolved Issues in the v3.3 Release

SAR	Description
73270	The configuration GUI has been updated to verify that the generic settings for FIFO sizes are consistent with other parameter settings.
73352	If TFIFODEPTH or RFIFODEPTH are set to 12, VHDL code may fail in Simulation and Synthesis, depending on the exact version of ModelSim® and Synplicity® used. The VHDL code has been updated to avoid this problem.
73578	When an interrupt acknowledge occurs (a write to CSR5), the core deactivates its interrupt out and then reasserts it a clock cycle later if there are still pending interrupts. This behavior is not desirable because it causes additional events on the interrupt line. The core has been modified so the interrupt output is only deasserted when all interrupts have been acknowledged.
73505	When the core is configured in 16-bit mode and receives a nonaligned frame, the following frame is not processed correctly even though that frame is correctly received. This issue has been resolved.

Resolved Issues in the v3.2 Release

Table 4 lists the Software Action Requests (SARs) that were resolved in the Core10100 v3.2 release.

Table 4 · Resolved Issues in the v3.2 Release

SAR	Description
72579	The Verification testbench will not invoke correctly when using Libero IDE v8.1. This has been resolved with updates to the core packaging.
72259	If a soft reset is performed when no receive or transmit clocks are present, the core will lock in an internal reset mode until the receive and transmit clocks are present. Some MII PHY devices disable the receive clock when no Ethernet cable is detected, causing this failure mechanism. When in the internal reset mode, the CSR registers will not be written. This has been fixed in the v3.2 release. Resets are no longer sensitive to the receive and transmit clocks.
72180	The AHB version of the core can, if incorrectly configured, initiate a multi-cycle AHB burst transfer with HBURST set to 000, indicating a single-word transfer. To prevent this protocol violation, the core now sets HBURST to 001 in all cases, indicating a burst of undefined length.
72117	CoreConsole incorrectly connected up the HBUSREQ and HGRANT signals when auto stitching the core. This issue has been fixed.
72128	The cataloging data used for CoreConsole and Libero IDE has been corrected.

Resolved Issues in the v3.1 Release

Table 5 lists the Software Action Requests (SARs) that were resolved in the Core10100 v3.1 release.

Table 5 · Resolved Issues in the v3.1 Release

SAR	Description
59757	In CoreConsole, the user can now export the handbook by right-clicking when Core10100 is selected in the CoreConsole core selection window.
59798 61767	The CoreConsole / Libero IDE design flow now correctly handles configuration with nonstandard address and data bus widths.
60150 61200 61206	Handbook corrections: Table 4-1 CSR1 and CSR2 reset values should be zero. Tables 4-27 and 4-28 show RX and TX descriptors as byte-wide. Figure 5-2 and 5-3 have incorrectly named signals.

Resolved Issues in the v3.0 Release

Table 6 lists the SARs that were resolved in the Core10100 v3.0 release.

Table 6 · Resolved Issues in the v3.0 Release

SAR	Description
56860	Width mismatch in tism module
57010	Core10100 does not receive packet lengths of non-multiples of data width.
57013	Receive side hangs in 16-bit mode when packet size is odd and >60.

Known Issues and Workarounds

Table 7 lists the known issues and the associated SARs.

Table 7 · Known Issues and Workarounds

SAR	Description
59797	During testing at the University of New Hampshire IEEE Fast Ethernet Interoperability Lab, it was identified that the re-transmit timing on the 11th attempt of the half-duplex backoff algorithm is more aggressive than a uniform distribution. This does not affect the core operation. All other tests passed.

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