
PCI Compliance Checklist

Actel CorePCIF v2.02 January 2006

Revision 2.2

Device is: Reserved ()
Device Address: 0x80000000
Vendor ID: 0x11AA

Device ID: 0x6004

Component Configuration Checklist

Test	Description	Result
CO_01	Does each PCI resource have a configuration space based on the 256 byte template defined in section 6.1., with a predefined 64 byte header and a 192 byte device specific region?	Yes ✓ No N/A
CO_02	Do all functions in the device support the Vendor ID, Device ID, Command, Status, Header Type and Class Code fields in the header? See figure 6-1.	Yes ✓ No N/A
CO_03	Is the configuration space available for access at all times?	Yes ✓ No N/A
CO_04	Are writes to reserved registers or read only bits completed normally and the data discard?	Yes ✓ No N/A
CO_05	Are reads to reserved or unimplemented registers, or bits, completed normally and a data value of 0 returned?	Yes ✓ No N/A
CO_06	Is the Vendor ID a number allocated by the PCI SIG?	Yes ✓ No N/A
CO_07	Does the Header Type field have a valid encoding?	Yes ✓ No N/A
CO_08	Do multi-byte transactions access the appropriate registers and are the registers in "little endian" order?	Yes ✓ No N/A
CO_09	Are all READ ONLY register values within legal ranges? For example, the interrupt pin register must only contain values 0-4.	Yes ✓ No N/A
CO_09	Vendor ID Implementation .	OK
CO_09	Latency_Timer Implementation .	OK
CO_09	Interrupt_Line Implementation .	OK
CO_10	Is the class code in compliance with the definition in Appendix D?	Yes ✓ No N/A
CO_10	Base Class is :	Simple communication controllers
CO_10	SubBase Class is :	Other communications device
CO_11	Is the predefined header portion of configuration space accessible as bytes, words, and dwords?	Yes ✓ No N/A
CO_12	Is the device a multifunction device?	Yes No ✓ N/A
CO_13	If the device is multifunction, are configuration space accesses to unimplemented function ignored.	Yes No N/A ✓
CO_14	Subsystem ID and Subsystem Vendor ID fields are:	
CO_14	Loaded and valid prior to any system software accessing these fields including after boot and resuming from a sleeping state:	Yes ✓ No N/A
CO_14	Not initialized by Expansion ROM code. Not Verified : The TA700_TA800 cannot implement this test .	
CO_15	Is bit 4 of the status register hardwired to 1?	Yes ✓ No N/A
CO_15	Is the Capabilities List pointer (offset 34h) implemented?	Yes ✓ No N/A
	Which capabilities are implemented (please list the Capability IDs in hex) 1 - Capability ID: 09	
CO_16	A capability list is used to indicate support:	Yes No N/A ✓
CO_16	If the device can generate 64-bit addresses as a master, then the MSI Message Address Upper register is implemented.	Yes No N/A ✓
CO_16	If the function is enabled for generating MSI (bit 0 in MSI Message Control = 1), then the functions INTX pin is not used:	Yes No N/A ✓

Indicate either N/A (Not Applicable) or Implemented by placing a check in the appropriate box. Grayed areas indicate invalid selections.

Location	Name	Required/Optional	N/A	Implemented
00h - 01h	Vendor ID	Required		X
02h - 03h	Device ID	Required		X
04h - 05h	Command	Required		X
06h - 07h	Status	Required		X
08h	Revision Id	Required		X
09h - 0Bh	Class Code	Required		X
0Ch	Cache Line Size	Required by master devices/functions that can generate Memory Write and Invalidate	X	
0Dh	Latency Timer	Required by master devices/functions that can burst more than two data phases	X	
0Eh	Header Type	If the device is multi-functional, then bit 7 must be set to a 1. The remaining bits are required to have a defined value.		X
0Fh	BIST	Optional(Built in self test).	X	
10h - 13h	Base Address 0	1 or more required for any address allocation.		X
14h - 17h	Base Address 1	1 or more required for any address allocation.	X	
18h - 1Bh	Base Address 2	1 or more required for any address allocation.	X	
1Ch - 1Fh	Base Address 3	1 or more required for any address allocation.	X	
20h - 23h	Base Address 4	1 or more required for any address allocation.	X	
24h - 27h	Base Address 5	1 or more required for any address allocation.	X	
28h - 2Bh	Cardbus CIS Pointer	Optional	X	
2Ch - 2Dh	Subsystem Vendor ID	Required		X
2Eh - 2Fh	Subsystem ID	Required		X
30h - 33h	Expansion ROM Base Address	Required for devices/functions that have expansion ROM	X	
34h	Capabilities Pointer	Optional		HardWire
35h - 37h	Reserved			X
38h - 3Bh	Reserved			X
3Ch	Interrupt Line	Required by devices/functions that use an interrupt pin		X
3Dh	Interrupt Pin	Required by devices/functions that use an interrupt pin		X
3Eh	Min_Gnt	Optional	X	
3Fh	Max_Lat	Optional	X	

Table 1 - Implementation of Configuration Space Header.

In the following tables for Command and Status Registers, an "x" in the "Implemented" column, indicates that applying the bit is appropriate. "N/A" indicates that applying the bit is not applicable, but must return a 0 when read.

Location	Name	Required/Optional	N/A	Implemented
0	I/O Space	(T) Required if device/function has registers mapped into I/O space		X
1	Memory Space	(T) Required if device/function responds to memory space accesses		X
2	Bus Master	(M) Required		X
3	Special Cycle	(T) Required for devices/functions that can respond to Special Cycles	X	
4	Memory Write and Invalidate Enable	(M) Required for devices/functions that generate Memory Write and Invalidate cycles	X	
5	VGA Palette snoop	(T) Required for VGA or graphical devices/functions that snoop VGA color palette	X	
6	Parity Error Response	Required unless exempted per section 3.7.2		X
7	Wait cycle control	Optional	X	
8	SERR# enable	Required if device/function has SERR# pin		X
9	Fast Back-to-Back Enable	(M) Required if Master device/function can support fast back-to-back cycles among different targets	X	
10-15	Reserved			

Table 2 - Implementation of Command registers Bits

(T) Required for Target Device.
(M) Required for Master Device.
N/A Not Applicable.

Device Control

Test	Description	Result
DC_01	When the command register is loaded with a 0000h is the device/function logically disconnected from the PCI, with the exception of configuration accesses? (Devices in BOOT code path are exempt).	Yes ✓ No N/A
DC_02	Is the device/function disabled after the assertion of PCI RST#? (Devices in BOOT code path are exempt).	Yes No ✓ N/A

Device Status

Bit	Name	Required/Optional	N/A	Implemented
0-3	Reserved	Required		X
4	Capabilities List	Optional	X	
5	66Mhz Capable	Required for 66MHZ capable devices	X	
6	Reserved	Required		X
7	Fast back-to-back capable	(T) Optional		X
8	Data Parity Detected	(M) Required	X	
9-10	DEVSEL# Timing	(T) Required		Reserved
11	Signaled Target Abort	(T) Required for devices/functions that are capable of signaling target abort		Unknown
12	Received Target Abort	(M) Required		Unknown
13	Received Master Abort	(M) Required		*
14	Signaled System Error	Required for devices/functions that are Capable of asserting SERR#		Unknown
15	Detected Parity Error	Required unless exempted per section3,7,2		Unknown

Table 3 - Implementation Requirements for Status Register Bits

- (T) Required for Target Device.
(M) Required for Master Device.
N/A Not Applicable.
(*) This test is not implemented in this version.

Test	Description	Result
DS_01	Do all implemented read/write bits in the Status reset to 0?	Yes ✓ No N/A
DS_02	Are read/write bits set to a 1 exclusively by the device/function?	Yes ✓ No N/A
DS_03	Are read/write bits reset to a 0 when PCI RST# is asserted?	Yes ✓ No N/A
DS_04	Are read/write bits reset to a 0 by writing a 1 to the bit?	Yes ✓ No N/A

Base Addresses

Register	N/A	I/O	Memory	Register Value	Register Request Space
Base Address 0			X	0X00000000	67108864
Base Address 1			X	0X00000000	8192
Base Address 2			X	0X00000000	256
Base Address 3	X			0X00000000	0
Base Address 4	X			0X00000000	0
Base Address 5	X			0X00000000	0
Expansion ROM Base Address	X			0X00000000	0

Table 4 - Implementation of Base Address register

* Upper 32 Bit of a 64 Bit address.

Base Addresses

Test	Description	Result
BA_01	If the device/function uses expansion ROM, does it implement the Expansion ROM Base Address Register?	Yes No N/A ✓
BA_02	Do all Base Address registers asking for IO space request 256 bytes or less?	N/A
BA_03	If the device/function has an Expansion ROM Base Address register, does the memory enable bit in the Command register have precedence over the enable bit in the Expansion ROM base Address register?	Yes No N/A ✓
BA_04	Does the device/function use any address space (memory or IO) other than that assigned using Base Address registers? (i.e.; Does the device/function hard-decode any addresses?) Note: If the answer is yes, you must list decoded addresses as explanations at the end of this section.	No
BA_05	Does the device/function decode all 32-bits of I/O space?	Yes No N/A ✓
BA_06	If the device/function has an Expansion ROM Base Address register, is the size of the memory space requested 16MB or smaller?	Yes No N/A ✓

GENERAL COMPONENT PROTOCOL CHECKLIST(TARGET)

Test	Description	Result
TP_01	All sustained Tri-State signals are driven high for one clock before being Tri-States (2.1). Not Verified: The TA700_TA800 cannot implement this test .	
TP_02	IUT never reports PERR# until it has claimed the cycle and completed a data phase. (2.2.5)	Yes ✓ No N/A
TP_03	IUT never aliases reserved commands with other commands. (3.1.1)	Yes ✓ No N/A
TP_04	32-bit addressable IUT treats DUAL command as reserved. (3.1.1)	Yes ✓ No N/A
TP_05	Once IUT has asserted TRDY# it never changes TRDY# until the data phase completes. (3.2.1)	Yes ✓ No N/A
TP_06	Once IUT has asserted TRDY# it never changes DEVSEL# until the data phase completes. (3.2.1)	Yes ✓ No N/A
TP_07	Once IUT has asserted TRDY# it never changes STOP# until the data phase completes. (3.2.1)	Yes ✓ No N/A
TP_08	Once IUT has asserted STOP# it never changes STOP# until the data phase completes. (3.2.1)	Yes ✓ No N/A
TP_09	Once IUT has asserted STOP# it never changes TRDY# until the data phase completes. (3.2.1)	Yes ✓ No N/A
TP_10	Once IUT has asserted STOP# it never changes DEVSEL# until the data phase completes. (3.2.1)	Yes ✓ No N/A
TP_11	IUT only transfers data when both IRDY# and TRDY# are asserted on the same rising clock edge (3.2.1). Not Verified: The TA700_TA800 cannot implement this test .	
TP_12	IUT always asserts TRDY# when data is valid on a read cycle. (3.2.1)	Yes ✓ No N/A
TP_13	IUT always signals target-abort when unable to complete the entire I/O access as defined by the byte enables. (3.2.2)	Yes No N/A ✓
TP_14	IUT never responds to reserved encodings. (3.2.2) Not Verified: The TA700_TA800 cannot implement this test .	
TP_15	IUT always ignores configuration command unless IDSEL# is asserted and AD(1:0) are '00'. (3.2.2)	Yes ✓ No N/A
TP_16	IUT always disconnects after the first data phase when reserved burst mode is detected. (3.2.2)	Yes ✓ No N/A
TP_17	The IUT's AD lines are driven to stable values during every address and data phase. (3.2.4)	Yes ✓ No N/A
TP_19	IUT never asserts TRDY# during turnaround cycle on a read. (3.3.1)	Yes ✓ No N/A
TP_20	IUT always deasserts TRDY#, STOP#, and DEVSEL# the clock following the completion of the last data phase. (3.3.3.2)	Yes ✓ No N/A
TP_21	IUT always signals disconnect when burst crosses resource boundary. (3.3.3.2)	Yes ✓ No N/A
TP_22	IUT always deasserts STOP# the cycle immediately following FRAME# being deasserted. (3.3.3.2.1)	Yes ✓ No N/A
TP_23	Once the IUT has asserted STOP# it never deasserts STOP# until FRAME# is negated. (3.3.3.2.1)	Yes ✓ No N/A
TP_24	IUT always deasserts TRDY# before signaling target-abort. (3.3.3.2.1)	Yes No N/A ✓
TP_25	IUT never deasserts STOP# and continues the transaction. (3.3.3.2.1)	Yes ✓ No N/A
TP_26	IUT always completes initial data phase within 16 clocks. If system is operating in run-time(i.e. more than 2**25 clocks after deassertion of RST#). (3.5.1.1) NOTE. The test design has DISABLE_WDOG set TRUE allowing the core to violate this specification. It is required as the SDRAM memory interface sometimes takes>16 clocks to return the first word	Yes No ✓ N/A
TP_28	IUT always issues DEVSEL# before any other response. (3.7.1)	Yes ✓ No N/A
TP_29	Once IUT has asserted DEVSEL# it never deasserts DEVSEL# until the	Yes ✓ No N/A

	last data phase has competed except to signal target-abort. (3.7.1)		
TP_30	IUT never responds to special cycles. (3.7.2)	Yes	✓ No N/A
TP_31	IUT always drives PAR within one clock of C/BE# and AD being driven. (3.8.1)	Yes	✓ No N/A
TP_32	IUT always drives PAR such that the number of '1's on AD(0:31), C/BE(3:0) and PAR equals an even number. (3.8.1)	Yes	✓ No N/A
TP_33	If IUT is accessed during initialization-time (time from RST# is deasserted and 2*25 clocks later), IUT responds to reacts the access by:		
TP_33	Completing the initial data phase within 16 clocks:	Yes	✓ No N/A
TP_33	Ignoring the access:	Yes	No ✓ N/A
TP_33	Claim the access and hold in wait states (completing within 2**25 clocks):	Yes	No ✓ N/A
TP_33	Claim the access and terminate with Retry:	Yes	No ✓ N/A
TP_34	After terminating a memory write transaction with Retry, IUT will be ready to complete at least one data phase of a memory write within 334 clocks for 33MHz devices and 668 clocks for 66MHz devices.	Yes	No N/A ✓