Introduction to

SMARTFUSION™
Intelligent Mixed-Signal FPGA

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September 8th, 2010
Agenda

- Introduction to SmartFusion
- Deeper Look inside SmartFusion
- Benefits & Examples
- Software & Eco-System
- Hardware Kits & Solutions
SmartFusion: Innovative, Intelligent, Integration

- Proven FPGA fabric
- Complete ARM® Cortex™-M3 MCU subsystem...& it’s ‘hard’
- Programmable analog
- In a flash-based device
- In production now!

Offers full customization, IP protection and ease-of-use
### The Actel Embedded Advantage

<table>
<thead>
<tr>
<th>Flash-based FPGA</th>
<th>SRAM-based FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM Cortex-M3 processor with its <strong>own</strong> embedded flash memory</td>
<td>Needs <strong>external</strong> flash memory</td>
</tr>
<tr>
<td>On-chip nonvolatile FPGA configuration</td>
<td>Needs external configuration devices</td>
</tr>
<tr>
<td><strong>High-voltage</strong> analog co-exists with digital circuits</td>
<td>Standard CMOS process <strong>not conducive</strong> to high voltage analog</td>
</tr>
</tbody>
</table>

**Flash Technology Enables Innovative, Intelligent Integration**
Customer Engagement To-Date: Some Applications

Battery Operated EKG/ECG

Servers and Switches

Ind controllers: Motion, Process & Safety

Synchronized Train Computers

System Management for ATCA boards

Target Applications
- System Management
- Power Management
- Motor Control
- Industrial Networking
- ….and more
An Inside Look at SmartFusion
No-Compromise FPGA Fabric

- Proven flash-based FPGA fabric
  - 60,000 to 500,000 system gates
  - 350 MHz system performance
  - Embedded SRAMs and FIFOs

- Ultimate Differentiator
  - Off load some often used or CPU intensive function into fabric
  - Add additional peripherals to meet design needs
No-Compromise Microcontroller Subsystem (MSS)

- 100 MHz 32-bit ARM Cortex-M3 processor
- Bus matrix with up to 16 Gbps throughput
- 10/100 Ethernet MAC
- SPI, I²C, UART, 32-bit Timers
- Up to 512 KB flash and 64 KB of SRAM
- External memory controller
- 8-channel DMA controller
- Up to 41 MSS I/Os
Cortex-M3 Processor Feature Summary

Wake-Up Interrupt Controller:
- Low gate count
- Configurable Number of Interrupts
- Suitable for separate power domain

Configurable Interrupt Controller:
- 1:240 Interrupts
- 1:255 Priority Levels
- NMI & SysTick

Central Core:
- 1.25 DMIPS/MHz
- Thumb-2 / Thumb ISA
- Hardware Divide 1cycle Multiply

ETM (Optional)

MPU (Optional)
- 8-Region Memory Protection Unit

ITM (Optional)

Debug Access Port:
- JTAG or Serial Wire

DWT (Optional)
- 4x Data Watchpoints & Event Monitors

FPB (Optional)
- 8x Hardware Breakpoints w. program patching

2x AHB-Lite Buses
- I_CODE (Instruction Code Bus)
- D_CODE (Data / Coefficients Code Bus)

1x AHB-Lite Buses
- SYSTEM (SRAM & Fast Peripherals)
- 1x APB Bus
- ARM Peripheral Bus (Internal & Slow Peripherals)
Cortex-M3 Implementation Options

- 150 Interrupts (151 including NMI)
  - 32 levels of interrupt priority

- Optional Memory Protection Unit (MPU) is present

- The Data Watchpoint and Trace (DWT) unit is configured to include data matching

- Optional Embedded Trace Macrocell (ETM) is not included

- The debug port implementation uses Serial Wire JTAG Debug Port (SWJ-DP) rather than Serial Wire Debug Port (SW-DP)
  - Enables JTAG or SW protocol to be used for debugging
SmartFusion AHB Bus Matrix

- **Masters**
  1. M3 – I/D Address/Data Bus
  2. M3 - System Address/Data Bus
  3. Ethernet MAC
  4. DMA
  5. FPGA Fabric Master

- **Slaves**
  1. S0 - Embedded SRAM block 0
  2. S1 - Embedded SRAM block 1
  3. S2 - Embedded eNVM block
  4. S3 - External Memory Interface
  5. S4 - APB_2
     - ACE
  6. S5 - Fabric Slave
  7. S6 - APB_0
     - SPI, I2C, UART, IAP, FROM
  8. S7 - APB_1
     - SPI, I2C, UART, Timer 1, Timer 2
External Memory Controller

- 2 Chip selects, each addressing 64 MB address space
  - Programmable timing for each chip select
- 8 and 16 bit data bus
- Asynchronous Memory Support:
  - Static Random Access Memory (SRAM)
  - NOR Flash Memory
  - PSRAM (async mode)
- Synchronous Memory Support:
  - Synchronous Static Random Access Memory (SSRAM)
- Slave on the AHB Bus Matrix
  - Can be used by any Master on the bus
- I/O Pads multiplexed with FPGA I/O signals
Programmable Analog

- Analog compute engine (ACE) offloads CPU from analog tasks
- Voltage, current and temp monitors
- 12-bit (SAR) ADCs @ up to 600 Ksps
- Sigma-Delta DACs
- Up to ten 15 ns high-speed comparators
- Up to 32 analog inputs and 3 outputs
Typical SmartFusion analog building block: 1 ADC, 1 DAC, 2 SCBs
Programmable Analog: A Closer Look

SmartFusion analog building block: 1 ADC, 1 DAC, 2 SCBs
(A2F200 has 2 of these)

• SDD = Sigma-Delta DAC
• TM = temp. monitor
• CM = current monitor
• ABPS = active bi-polar pre-scaler
Innovative Intelligent Integration
In-Application Programming (IAP)

- APB bus slave under control of Cortex-M3
  - Basically an APB slave interface into Fabric TAP controller
- Interface to internal FPGA programming circuitry
- New FPGA image can come from any MSS port
  - Store redundant images in SPI flash memory
Clock Sources

- 100 MHz RC oscillator
  - ± 1% 0 to 85 C
  - No external components required
  - Always on except for Sleep mode

- Main Oscillator
  - 32KHz to 20 MHz
  - With External Crystal

- Low Power Crystal Oscillator
  - Designed to work with a low-power 32 KHz watch crystal
  - Can be powered externally by a CR2032 lithium cell
  - Can be enabled and disabled by setting and clearing bit 0 of the CTRL_STAT_REG in the RTC
Clock Hierarchy
# SmartFusion Family: Key Features

<table>
<thead>
<tr>
<th>Device</th>
<th>A2F060*</th>
<th>A2F200</th>
<th>A2F500</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Gates (Kgates)</td>
<td>60</td>
<td>200</td>
<td>500</td>
</tr>
<tr>
<td>Tiles (D-flip-flops)</td>
<td>1,536</td>
<td>4,608</td>
<td>11,520</td>
</tr>
<tr>
<td>RAM Blocks (4,608 bits)</td>
<td>8</td>
<td>8</td>
<td>24</td>
</tr>
<tr>
<td>MSS</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>10/100 Ethernet MAC</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>eNVM</td>
<td>128K</td>
<td>256K</td>
<td>512K</td>
</tr>
<tr>
<td>eSRAM</td>
<td>16K</td>
<td>64K</td>
<td>64K</td>
</tr>
<tr>
<td>Analog Compute Engine (ACE)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>ADCs (8-/10-/12-bit SAR)</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>DACs (12-bit Sig-Del)</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Comparators</td>
<td>2</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Current Monitors</td>
<td>1</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Temperature Monitors</td>
<td>1</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Bipolar HV Monitors</td>
<td>2</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Direct Analog Input</td>
<td>8</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td><strong>Total Analog Input</strong></td>
<td>12</td>
<td>24</td>
<td>32</td>
</tr>
<tr>
<td><strong>Total Analog Output</strong></td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>MSS I/O</td>
<td>25</td>
<td>41</td>
<td>41</td>
</tr>
<tr>
<td>FPGA I/O</td>
<td>66</td>
<td>94</td>
<td>128</td>
</tr>
<tr>
<td><strong>Total I/O</strong></td>
<td><strong>104</strong></td>
<td><strong>161</strong></td>
<td><strong>204</strong></td>
</tr>
</tbody>
</table>

* Under definition. Subject to change.

**MCU Sub-System (MSS)**

- Analog Front End
- ProASIC3 Fabric

**MSS Common to all Family Members**

- Cortex M3 (100MHz)
- 2 – SPI
- 2 – UART
- 2 – I2C
- 2 – 32-bit Timers
- DMA
- Watch Dog
- RTC
- External Memory Controller

**Availability:**
- Now: A2F200
- Now: A2F500
- Nov’10: A2F060
# SmartFusion Package Offering

<table>
<thead>
<tr>
<th>Device</th>
<th>A2F060*</th>
<th>A2F200</th>
<th>A2F500</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS288 (11x11; 0.5mm pitch)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FG256 (17x17 mm; 1mm pitch)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FG484 (23 x 23 mm; 1mm pitch)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Under definition. Subject to change.

- **Packages currently under consideration**
  - 144TQFP (20 mm x 20mm; 0.5mm pitch; 1.4mm height)
SmartFusion Multi-Function I/Os

<table>
<thead>
<tr>
<th>Device</th>
<th>A2F200</th>
<th>484FBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total Analog Inputs</strong></td>
<td>24</td>
<td></td>
</tr>
<tr>
<td><strong>Total Analog Outputs</strong></td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>MSS I/Os&lt;sup&gt;1,2,3&lt;/sup&gt;</td>
<td>41</td>
<td></td>
</tr>
<tr>
<td>FPGA I/Os&lt;sup&gt;4&lt;/sup&gt;</td>
<td>94</td>
<td></td>
</tr>
<tr>
<td><strong>Total I/Os</strong></td>
<td>161</td>
<td></td>
</tr>
</tbody>
</table>

1. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS
2. 9 MSS I/Os are primarily for 10/00 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design.
3. 16 MSS I/Os shared between I2C/UART/SPI and GPIOs
4. 50 of 94 FPGA I/Os are multiplexed as EMC (Ext Mem Controller IOs)
Why SmartFusion is a Smart Decision?
Why SmartFusion is a Smart Decision

- No-compromise integration
  - Complete ARM Cortex-M3 subsystem running at 100 MHz
  - Proven flash-based FPGA fabric
  - Programmable high-voltage analog

- Full customization
  - Design the exact system you need
  - Hardware and software co-design

- IP protection
  - FlashLock® technology with 128-bit AES encryption

- Ease-of-use
  - Independent design flows for hardware and software design

- Reliability
- Smaller footprint
- Fewer vendors
- Lower TCO

- Extend product life
- In-field upgrades
- One platform for multiple products

Protection Against:
- Overbuilding
- Cloning
- Tampering

- GUI based design
- Complete Eco-System
- Industry leading partners
System Management

Fewer components, less board space, fewer vendors
System Management

Fewer components, less board space, fewer vendors
SmartFusion Offers Unparalleled IP Protection

- Microcontroller and FPGA interface not exposed
- No bitstream at boot-up
- FlashLock protects against tampering and reprogramming
- AES-encrypted in-system programming
- Protects against overbuilding with programmable device key
Motor Control: Integration Benefit

SmartFusion replaces:
- ARM9
- SRAM FPGA
- Analog acquisition device array
SmartFusion:
Software & Eco-System
SmartFusion Design Environment

- Full-featured traditional FPGA design flow
- Industry-leading software IDEs for embedded design
- Simulation, timing and power analysis reduce debug time
- Debug through FlashPro or standard RealView® header
MSS Configurator

- Configure the MSS peripherals and I/Os
- Create or import hardware configuration
- Automatically generate drivers for peripherals
- Configure programmable analog components

*MSS configurator enables co-design between multiple users*
SmartFusion stack accelerates application development
Industry Leading Ecosystem Partners

- Actel
  - HAL, drivers and IDE
- ARM Cortex-M3 processor
  - Leverage ARM ecosystem
- GNU, Keil and IAR
  - Compilers and debuggers
- Micrium
  - RTOS, TCP/IP and middleware
- Mentor and Synopsys
  - Synthesis and simulation
SmartFusion: Hardware & Solution Kits
Evaluation and Development Kits

- $99 – evaluate SmartFusion
- Evaluate and debug the entire system
- Tutorials and sample code
to accelerate learning curve

- $999 Development Kit
- More on-board memory
- I/O expansion header
- External memory expansion header
- Industrial automation interfaces
Mixed-Signal Power Management (MPM)

- Demonstrates power management using SmartFusion
  - Power-up, monitor, voltage trim, data log and power-down
  - All configurable via standalone GUI tool on PC
  - Configuration changes via changing register values

- SmartFusion MPM solution includes
  - MPM daughter card: attaches to Evaluation kit
  - SmartFusion MPM design example
  - Standalone graphical configurator PC tool: Simplifies analog design
SmartFusion-based solutions for the xTCA™ market

- IPM Controllers (IPMCs) for ATCA boards
- Carrier IPMCs for ATCA AMC carrier boards
- Module Management Controllers for AMC modules

a dominant supplier of hardware platform management
Motor Control: Co-processing Benefit

Efficient co-processing performance between FPGA and MCU
SmartFusion Motor Control Partners

- Power and Control Design, Incorporated (PCD)
  www.powerandcontroldesign.com

- TRINAMIC Motion Control GmbH & Co.
  www.trinamic.com
Summary

- SmartFusion is the only device of its kind
  - FPGA + MCU subsystem + programmable analog

- Innovative, intelligent, integration made possible by Actel’s unique flash technology

- Easy-to-use tools for both FPGA and embedded designers

- In production now

For more information: www.actel.com/SmartFusion
For Hands-on & Online Trainings: www.actel.com/training