Designing for Low Power with Programmable System Solutions

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Overview

- Why is power a problem?
- What can FPGAs do?
- Are we safe now?
- What else can FPGAs do?
- Summary
The Shrink and Its Impact

- Speed
- Cost
- Power
Static power increases significantly at <100nm geometries

Sub-threshold Leakage
- Raising VT helps, but there’s a limit
- Strain helps, but that’s already been done
- Worsens with reduced voltage

Power and speed at odds

Power is becoming a market limiter

Source: Int’l Technology Roadmap for Semiconductors (ITRS)
What about Dynamic Power?

- Power = CV^2F

- C - Low K helps, but increasing due to higher densities

- V - Fell previously, but now same

- F - Increasing steadily
Semiconductor Fab Cost Trend

- Rising Fab Cost

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Source: UMC
Trends Continue to Drive Demand for Low-power FPGAs

- Portable and battery-operated electronics proliferation
- Hyper-competitive markets with shorter product lifecycles and evolving standards
  - Increasing need for interfacing, bridging and control
- Power budgets tighten
  - Features, performance and complexity grow, but not at expense of draining the battery or increasing footprint
- Static power consumption and low-power modes most important for portables
Flash’s Fundamental Advantage

Typical Competitors SRAM Cell – 6T
- Substantial leakage per cell
- High static current

Flash Cell – 1T
- Negligible leakage per cell
- Ultra-low static current
What have we done?

Technology and Design

- Integrate flash and high-speed embedded logic process
- Deploy low power Vt options, multiple thresholds
- Single supply for core and I/Os
  - As low as 1.2V
- Seamless low-power implementation modes
  - Static, Flash*Freeze
- Feature-rich
  - RAM, PLL, I/O standards, Cortex-M1
Power-Aware Tools

- **Power-driven Layout**
  - Yields lowest power consumption possible
  - Reduces dynamic power by 30%

- **SmartPower**
  - Create power profiles based on functional modes
  - Cycle-accurate analysis
  - Spurious transitions analysis
  - Battery life estimation tool
  - Enable variable voltage use modes
A Static Power Comparison

- **IGLOO PLUS 5µW**
- **Competitors**
  - Low-power CPLDs
  - SRAM-based, low-power PLDs
  - 10x higher power

### 30k system gates
- Competitor A: 59µW
- Competitor B: 52µW
- IGLOO PLUS: 5µW

### 60k system gates
- Competitor A: 90µW
- Competitor B: 58µW
- IGLOO PLUS: 10µW
Declare victory and go home
1.2% of electricity consumed in the US is used in server farms
Server Math

- Power for:

  - 100% Server
  - 60% Fan and Air Conditioning
  - 60% Switch, Router and Network

  220%

- i.e. Total Power = 2.2x Server Power
Industry Reacts with System Management Standards

- **Telecommunications Computing Architecture (TCA)**
  - Standards by PCI Industrial Computer Manufacturers Group (PICMG)

- **Advanced Telecommunications Computing Architecture (ATCA)**
  - Architecture for high-performance, high-density, packet-based systems
  - Current rev is PICMG 3.0 R2.0 ECN002 adopted April 2006

- **Advanced Mezzanine Card (AMC)**
  - Extends ATCAs high-bandwidth multi-protocol interface to hot-swappable modules for easy design, scaling and servicing
  - Current rev is PICMG AMC.0 R2.0 adopted November 2006
Industry System Management Standards (cont.)

- **MicroTCA (μTCA)**
  - Smaller form-factor chassis delivers central power management, lower cost, high availability
  - Current rev is PICMG MTCA.0 R1.0 adopted 06 July 2006

- **Intelligent Platform Management Interface (IPMI)**
  - Intelligent Platform Management Bus (IPMB) defines internal management bus for extending platform management within a chassis
  - Intelligent Chassis Management Bus (ICMB) defines external management bus between IPMI enabled systems
  - ATCA, AMC and MicroTCA all communicate using IPMI protocol
  - Current rev is IPMI v2.0 rev. 1.0 spec markup for IPMI v2.0/v1.5 errata rev 3 dated February 2006
Customers Need System Management

- **Manage power up**
  - power sequencing
  - status monitoring

- **Monitor sensors and report status, sensor data**
  - Temperature
  - Voltage
  - Current
  - Boot Status

- **Take immediate actions based on sensor readings**
  - Over/under-voltage
  - Current & temp

- **Communicate with system controllers/hubs**
  - Oversee system inventories
  - Implement system-level redundancy
  - Manage hot swap
  - Respond to management queries and commands
Integrated solution today with compelling features
Fusion system management solutions are here today

- System management includes following benefits:
  - Overall lower power, with intelligent power management
  - BOM reduction
- Fusion roadmap will continue to extend these benefits
Fusion Analog Features

- **Successive Approximation Register (SAR) ADC**
  - Up to 12 bit or 600 Ksps
  - Better than 1% total channel accuracy with calibration
  - Internal reference voltage
- **Built in sample and hold**
  - Increases accuracy of dynamic signals
- **Analog I/O**
  - ± 12 V Tolerant
  - Up to 30 channels input
  - Current monitor block
    - 2 mV resolution
  - Temperature monitor block
    - ±3°C accuracy
    - ±5°C Offset
  - MOSFET Gate driver output
    - Programmable drive strength
    - P and N channel devices
Fusion Flash Features

- **Flash memory 2 Mb density**
  - 1 – 4 blocks/device
  - Each 2 Mb array operates independently supporting multiple partitions
  - Small page size (1kb)
  - Independent JTAG access

- **Supports High performance**
  - 60 ns random access
  - Pipelined 10 ns access of sequential memory addresses

- **Flash Memory level:**
  - FPGA access
  - Password security
  - JTAG access for programming

- **Page level:**
  - JTAG read / write protection
  - Program/erase
  - Partition on page boundaries

- **Block level error detect:**
  - Single error correct
  - Double error detect
Comprehensive Clocking Resources

- **Fusion builds up clocking resources:**
  - On chip clock sources:
    - CCC (6) / PLLs (1 or 2)
    - RC oscillator
    - Crystal Oscillator
  - Real Time Counter (RTC)

- **Use Models**
  - Internal 100MHz RC oscillator
    - ±2% over l-temp range
  - Crystal OSC circuit
    - 32 KHz – 20 MHz
  - CCC/PLLs can multiply, divide, and phase shifts clock signals for user applications
    - Sources include: crystal Osc, RC Osc, or external clock
  - RTC enables low power standby mode
- Power-conscious design is becoming more critical
  - Not only choice of components, but power-smart design

- Actel is focused on attacking power consumption at chip and system levels with
  - Innovative low-power FPGAs and programmable system chips
  - Targeted FPGA-based reference designs and boards
  - Power optimization tools

- At 5µW, Actel’s IGLOO family is the low-power programmable logic leader