



# Synplify – Synthesis Frequently Asked Questions

Version 1.0

## Table of Contents

<b>Introduction to Synopsys Synplify .....</b>	<b>4</b>
1.    What does Synplify do? .....	4
2.    Which HDL language does Synplify support? .....	4
3.    Will Synplify accept manual instantiations of Actel macros? .....	4
4.    How does Synplify work with Actel tools? .....	4
<b>Licensing Download Installation .....</b>	<b>5</b>
5.    Where can I download the latest Synplify release? .....	5
6.    Which version of Synplify is released with the latest Libero IDE? .....	5
7.    How do I upgrade to the latest version of Synplify and use it in the Libero IDE Project Manager? .....	5
8.    Do I need a separate license to run Synplify in Libero IDE? .....	5
9.    Where and how do I get the license for Synplify? .....	5
10.   Why can't I run Synplify in batch mode? What license does it require? .....	5
11.   Why is my Synplify license not working? .....	6
12.   Can I use the Synplify license obtained from Actel to run any version of Synplify? .....	6
<b>Warnings/Error Messages .....</b>	<b>7</b>
13.   Warning: Top entity isn't set yet! .....	7
14.   Warnings on Register Pruning. ....	7
15.   @W: FP101  The design has 8 instantiated global buffers but allowed is only 6 .....	8
16.   Error: The profile for tool Synplify is interactive and you are running in batch mode: this tool cannot be invoked .....	8
17.   @E: CG103 : "C:\PATH\code.vhd":12:13:12:13 Expecting expression .....	9
18.   @E: Internal Error in m_proasic.exe .....	9
19.   @W: CD639 : "C:\Program Files\2PAC3\MSE\PAC3_j\viewdraw\PAC_3.vhd":306:11:306:17 Bit <0> of signal s15_cnt is undriven .....	9
20.   @W: BN269  Library ARC Pruning: Multiple bidi in cell BIBUF_LVDS. Pruning abandoned. ....	9
21.   Why has my logic block disappeared after synthesis? .....	9
<b>Attributes/Directives .....</b>	<b>10</b>
22.   How do I turn off automatic clock buffer usage in Synplify? .....	10
23.   Which attribute is used for preserving registers? .....	10
24.   Does syn_radhardlevel attribute support IGLOO and Fusion families? .....	10
25.   How do I "Disable serial optimization" in Synplify? .....	10
26.   How can I add an attribute in Synplify? .....	10
27.   How do I insert a clock buffer in my design? .....	11
28.   How do I increase the number of global clock buffers used in my design? .....	11
29.   Is there any way to preserve my logic if the output ports are not used in my design? ...	12
30.   Why is synthesis optimizing my high fanout net to buffered clock? .....	12
31.   How do I use the syn_encoding attribute for an FSM design? .....	12

---

32. Synplify generates a netlist that exceeds the maximum fanout of device, causing the netlist to fail compile.....	12
<b>RAM Inference .....</b>	<b>13</b>
33. Which Actel families do Synplify support for RAM inference? .....	13
34. Is RAM inference ON by default? .....	13
35. How can I turn off RAM inference in Synplify? .....	13
36. How do I make Synplify infer embedded RAM/ROM? .....	13
37. Why is my RAM RTL code inferring unwanted logic?.....	13
38. I cannot compile an existing design in a newer version of Designer?.....	13
<b>Area / Quality of Results .....</b>	<b>14</b>
39. Why does area usage increase in the new version of Synplify?.....	14
40. What kind of Area improvement technique is available in Synplify? .....	14
41. How do I disable area optimization? .....	14
42. How do I “Disable sequential optimization”?.....	15
<b>TMR Usage.....</b>	<b>16</b>
43. Which family is TMR supported through Synplify?.....	16
44. Why is TMR macro working in SX, but not in AX family? .....	16
45. How can I enable TMR for a SX-A device? .....	16
<b>Miscellaneous .....</b>	<b>17</b>
46. Which version of Synplify supports Nano products? .....	17
47. Which version of Synplify provides RTAX-DSP support? .....	17
48. I am having trouble using the HDL Analyst tool. ....	17
49. How do I create an IP core with the HDL files I have?.....	17
50. Why am I not seeing my new port list even after I updated the netlist? .....	17
51. Why doesn't my multicycle path constraint work? .....	17
52. Why is Synplify not using Global for Set/Reset signals? .....	17
53. Why does Synplify write out SDC clock constraints even for auto-constraints? .....	17
54. Why is my internal tristate logic not synthesized correctly? .....	18

# Introduction to Synopsys Synplify

## 1. What does Synplify do?

The Synplify and Synplify Pro products are logic synthesis tools for FPGAs (field programmable gate arrays) and CPLDs (complex programmable logic devices). The Synplify Pro tool is an advanced version of the Synplify tool, with many additional features for managing and optimizing complex FPGAs. Some additional features available in Synplify Pro are FSM explorer, FSM viewer, Register retiming, gated clock conversion etc.

These tools accept high-level input written in industry-standard hardware description languages (Verilog and VHDL), and using the Synplicity Behavior Extracting Synthesis Technology® (BEST™) algorithms, they convert the designs into small, high performance design netlists for popular technology vendors. They can also write VHDL and Verilog netlists after synthesis, which you can then simulate in order to verify functionality.

## 2. Which HDL language does Synplify support?

Verilog 95, Verilog 2001, System Verilog IEEE (P1800) standard and VHDL 93 are supported in Synplify. To check for the different language constructs supported refer to

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

## 3. Will Synplify accept manual instantiations of Actel macros?

Yes. Synplify contains built-in macro libraries for all of Actel's hard macros including logic gates, counters, flip flops, and I/Os. You can manually instantiate these macros in your Verilog and VHDL designs, and Synplify will pass them through to the output netlist.

## 4. How does Synplify work with Actel tools?

The Synopsys® Synplify Pro® AE synthesis tool is integrated into the Libero IDE, enabling you to target and fully optimize your HDL design for any Actel device. As with all other Libero IDE tools, you can launch Synplify Pro AE directly from the Libero IDE Project Manager.

Synplify Pro AE is the standard offering in Libero Gold and Libero Platinum editions. Synplify Pro AE is launched by invoking the executable specific in the Libero Tool Profile.

## Licensing Download Installation

### 5. Where can I download the latest Synplify release?

Synplify can be obtained by downloading and installing Libero IDE, or it can be downloaded as a standalone installation from

<http://www.actel.com/download/software/synplify/files.aspx>

### 6. Which version of Synplify is released with the latest Libero IDE?

The latest version of Libero IDE released is Libero 8.6 with Synplify Pro Actel Edition (AE) 2009.03A-2 included. The latest release information can be found at

<http://www.actel.com/download/software/libero/default.aspx>

### 7. How do I upgrade to the latest version of Synplify and use it in the Libero IDE Project Manager?

Download and install the latest version of Synplify from the Actel or Synopsys website, and change the synthesis settings in the Libero IDE Project Manager Tool Profile from the Libero Project->Profiles Menu.

### 8. Do I need a separate license to run Synplify in Libero IDE?

No. All Libero IDE Licenses except for the Libero-SA (Standalone) license includes a license for the Synplify software.

### 9. Where and how do I get the license for Synplify?

To apply for a free license, go to <http://www.actel.com/products/software/libero/licensing.aspx> and click the **Software Licenses and Registration System** link. You will need to input information, including the volume ID of your C drive. Make sure to apply with your C drive, even if that is not the drive you intend to install the software on. If you will be using a license type which is not free, please contact your local Actel Sales Office.

### 10. Why can't I run Synplify in batch mode? What license does it require?

From a command prompt, go to the directory where the project files are located and type the following:

```
synplify -batch -licensetype synplify_acteloem Tcl_script.tcl
```

```
synplify_pro -batch -licensetype synplifypro_acteloem Tcl_script.tcl
```

You must have a Platinum license to run Synplify in batch mode. Contact your local Actel sales representative to purchase a Platinum license.

## 11. Why is my Synplify license not working?

Perform the following checks on your license:

- a) Check if the license has expired.
- b) Check if the LM\_LICENSE\_FILE is set correctly as a windows user environment variable which points to the location of the Libero License.dat file.
- c) Is Libero IDE tool profile set to Synplify Pro?
- d) Check if the Synplify license feature is enabled in your license file.
- e) Look for the “synplifypro\_acteloem” feature line in license.dat and make sure the HostID is correct for the computer you are using.

```
FEATURE synplifypro_acteloem synplctyd 2005.158 20-feb-2009 uncounted  
\  
6DBA20564A500582CB62 VENDOR_STRING=actel_oem,nl \  
HOSTID=DISK_SERIAL_NUM=bc7b6ec2 \  
\
```

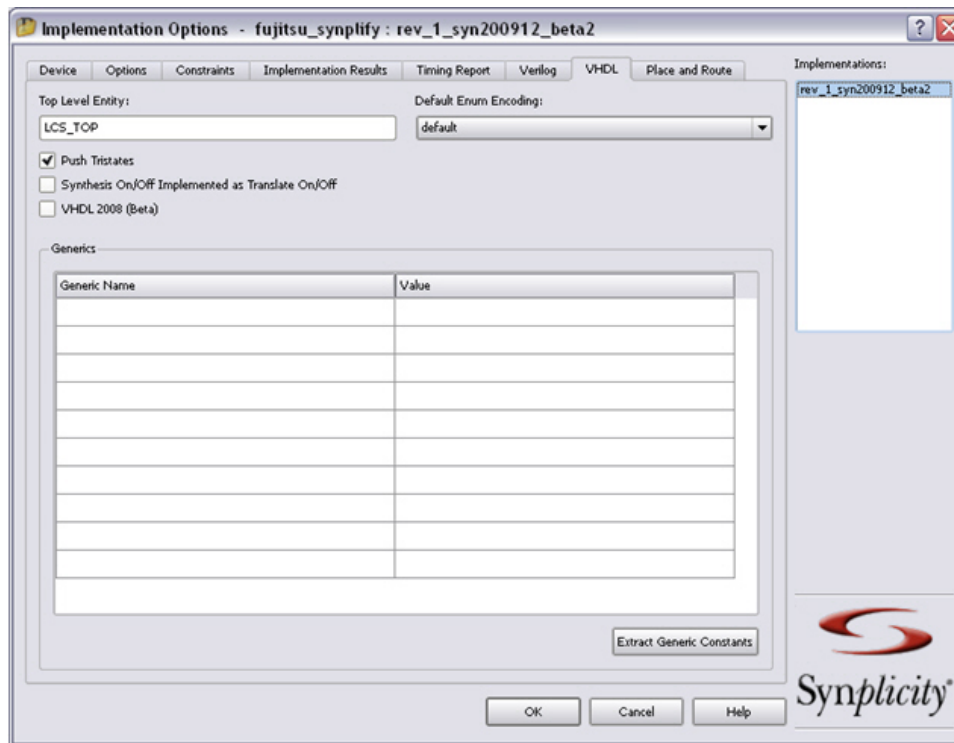
## 12. Can I use the Synplify license obtained from Actel to run any version of Synplify?

No, if you received a Synplify license from Actel, you will only be able to run Synplify AE (Actel Edition).

## Warnings/Error Messages

### 13. Warning: Top entity isn't set yet!

Synplify could not identify the top entity in your design, due to design complexity. You need to manually specify the top entity name in Synplify Implementation Options. Please see the figure below for an example.



### 14. Warnings on Register Pruning.

Synplify optimizes the design by pruning unused/duplicate registers/nets/blocks. You can manually control the amount of auto optimization by applying the following directives:

\*syn\_keep ensures that 1) a wire is kept during synthesis and 2) that no optimizations cross the wire. This directive is usually used to break unwanted optimizations and to ensure manually created replications. It works only on nets and combinational logic.

\*syn\_preserve ensures that registers are not optimized away.

\*syn\_noprune ensures that a black box is not optimized away when its outputs are unused (i.e., when its outputs do not drive any logic).

You can get more information on optimization control in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### 15. @W: FP101 |The design has 8 instantiated global buffers but allowed is only 6

@W: FP103 |User can use `syn_global_buffers` to increase the allowed global clock buffers to maximum 18

The warnings were created because Synplify identified more than 6 global macros instantiated in the design. The default maximum number of global nets allowed in Synplify is currently set to 6. So when the tool tried to use more than 6 for this design, it generated an error. You can manually increase this default limit to 8 (up to 18 in IGLOO/e, ProASIC3/E, and Fusion) by adding a synthesis attribute called “`syn_global_buffers`”.

For example:

```
module top (clk1, clk2, d1, d2, q1, q2, reset) /* synthesis
syn_global_buffers = 8 */;
```

.....

or

...

architecture behave of top is

```
attribute syn_global_buffers : integer;
```

```
attribute syn_global_buffers of behave : architecture is 8;
```

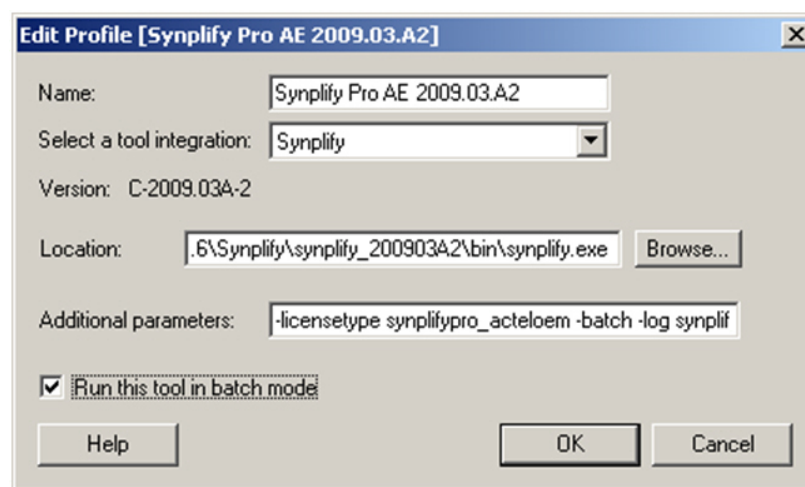
.....

For more information, refer to the Synplify Reference Manual at:

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### 16. Error: The profile for tool Synplify is interactive and you are running in batch mode: this tool cannot be invoked

You must have a Platinum license to run Synplify in batch mode. Contact your local Actel sales representative to purchase a Platinum license. You must also ensure that the Libero Synthesis Tool Profile is configured to launch Synplify in Batch Mode if you are invoking Synplify from within Libero IDE instead of directly at the command prompt. See the figure below:



**17. @E: CG103 : "C:\PATH\code.vhd":12:13:12:13|Expecting expression**

@E: CD488 : "C:\PATH\code.vhd":14:11:14:11|EOF in string literal

A comment following anything other than a semicolon or a new line is illegal in VHDL. Two hyphens mark the start of a comment, which is ignored by the VHDL compiler. A comment can be on a separate line or at the end of a line of VHDL code. The error is due to comments in some other part of the VHDL code.

**18. @E: Internal Error in m\_proasic.exe**

This is not an expected tool behavior. Please contact Synopsys Synplify support team for an explanation. You can also contact Actel Tech Support if you do not have a Synopsys Support Account.

**19. @W: CD639 : "C:\Program**

**Files\2PAC3MSE\PAC3\_j\viewdraw\PAC\_3.vhd":306:11:306:17|Bit <0> of signal s15\_cnt is undriven**

This warning is caused by a known issue explained in the following link:

<http://www.actel.com/kb/article.aspx?id=K139643>

Since the individual bits of a bus are renamed, Synplify gave warnings for unused bits with original names. Therefore, these warnings can be ignored if the design synthesized correctly.

**20. @W: BN269 |Library ARC Pruning: Multiple bidi in cell BIBUF\_LVDS. Pruning abandoned.**

This is an internal message from synthesis mapper and was supposed to display only in the development and debug mode of Synplify. The message was accidentally turned on in the production build produced by Synopsys. It can be safely ignored and it will likely not be displayed in future versions of Synplify.

**21. Why has my logic block disappeared after synthesis?**

Synplify optimizes away any logic block that does not have any external output port.

## Attributes/Directives

### **22. How do I turn off automatic clock buffer usage in Synplify?**

You can turn off automatic clock buffering for nets or specific input ports by using the `syn_noclockbuf` attribute. Set the Boolean value to 1 or true to turn off automatic clock buffering.

You can attach this attribute to a hard architecture or module whose hierarchy will not be dissolved during optimization of a port, or net.

More details on usage of the attribute can be found in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### **23. Which attribute is used for preserving registers?**

Use `syn_preserve` directive.

More details on this attribute can be found in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### **24. Does `syn_radhardlevel` attribute support IGLOO and Fusion families?**

No. `syn_radhardlevel` attribute is not supported in IGLOO and Fusion families. See questions 43 to 45 for more information about the TMR setting of the `syn_radhardlevel`.

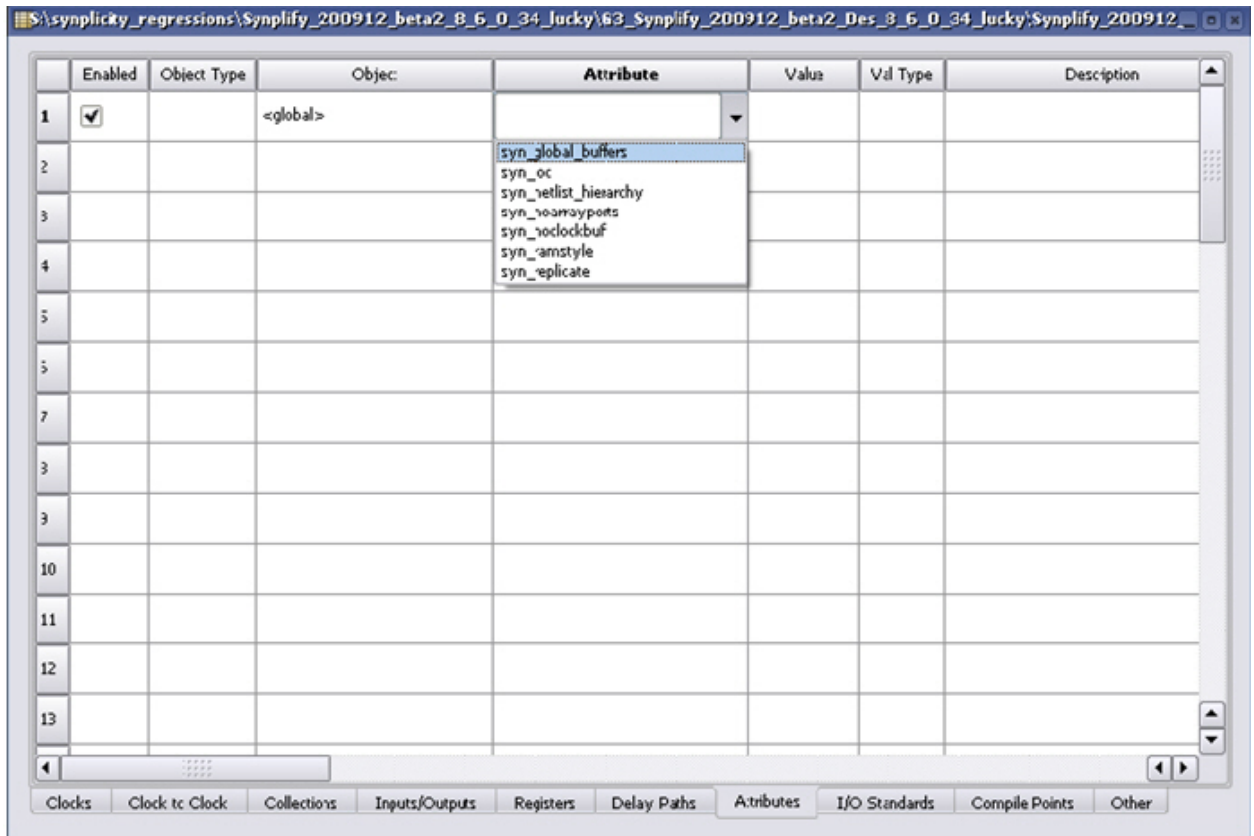
### **25. How do I “Disable serial optimization” in Synplify?**

Use `syn_preserve` directive.

### **26. How can I add an attribute in Synplify?**

- a. Launch Synplify from the Libero IDE Project Manager.
- b. In the Synplify toolbar, click the New Scope File icon; it looks like a spreadsheet.
- c. Click the Attributes tab at the bottom of the spreadsheet.

- d. Double-click in any of the attribute cells in the spreadsheet. You should see a pull-down menu with many attributes listed. You can select any of them, and fill in the required fields accordingly (as shown in the figure below).
- e. When you are done, save the files and close the Scope Editor.



## 27. How do I insert a clock buffer in my design?

Use `syn_insert_buffer` attribute to insert a clock buffer. The synthesis tool inserts a clock buffer according to the vendor-specific values you specify. The attribute can be applied on instances.

More details on usage of the attribute can be found in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

## 28. How do I increase the number of global clock buffers used in my design?

Use `syn_global_buffers` attribute in the SCOPE to specify the number of global buffers to be used in a design. It will be an integer between 0 and 18. More details this attribute can be found in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### 29. Is there any way to preserve my logic if the output ports are not used in my design?

Use `syn_noprune` attribute.

For example: `module syn_noprune (a,b,c,d,x,y); /* synthesis syn_noprune=1 */;`

More details on this attribute can be found in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### 30. Why is synthesis optimizing my high fanout net to buffered clock?

Use `syn_maxfan` to override the default (global) fanout guide for an individual input port, net, or register output. You set the default fanout guide for a design through the device panel on the Implementation Options dialog box or with the `set_option -fanout_limit` command in the project file. Use the `syn_maxfan` attribute to specify a different (local) value for individual I/Os.

More details on this attribute can be found in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### 31. How do I use the `syn_encoding` attribute for an FSM design?

The `syn_encoding` attribute overrides the default FSM Compiler encoding for a state machine. This attribute takes effect only when FSM Compiler is enabled. You can also use `syn_encoding` when you want to disable the FSM Compiler globally but there are a select number of state registers in your design that you want extracted. In this case, use this attribute with the `syn_state_machine` directive on for just those specific registers.

More details on this attribute can be found in the following document

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### 32. Synplify generates a netlist that exceeds the maximum fanout of device, causing the netlist to fail compile.

A CC macro is a flip-flop element built using two C-cells. A net driving the CLK or CLR port of a CC macro in reality is driving two cells. The hard fan-out limit on certain nets does not achieve the desired results because it fails to take this net doubling effect into account.

Include the `syn_maxfan` attribute in the RTL code to force Synplify to generate a valid netlist. Remember to reduce the max fanout limit value by one for every CC macro driven by the net. For example: Set the `syn_maxfan` limit to 12 for a net that is driving CC macros to keep the fanout at 24 or less.

## RAM Inference

### **33. Which Actel families do Synplify support for RAM inference?**

Synplify supports the Actel ProASIC, ProASIC PLUS, and ProASIC3 families in generating both single- and dual-port RAMs.

### **34. Is RAM inference ON by default?**

Yes. The synthesis tool automatically infers RAM.

### **35. How can I turn off RAM inference in Synplify?**

Use `syn_ramstyle` attribute and set its value to `registers`.

See the following document for more information

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### **36. How do I make Synplify infer embedded RAM/ROM?**

Use `syn_ramstyle` attribute and set its value to `block_ram`.

See the following document for more information

[http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf)

### **37. Why is my RAM RTL code inferring unwanted logic?**

It is a bug in Synplify and it has been resolved in Syn. 2009.06A version onwards.

### **38. I cannot compile an existing design in a newer version of Designer?**

There could be possible RAM/PLL configuration change. Please regenerate your RAM/PLL by opening the core configuration options from the Catalog in the Libero IDE Project Manager, and re-synthesize/compile/layout.

## Area / Quality of Results

### 39. Why does area usage increase in the new version of Synplify?

Synplify is designed to achieve better timing results in every new version. Unfortunately, the trade-off is often an area increase.

If you have already achieved timing requirement for your design, and all you wanted to do was to fit the design in a specific die, you can try the following methods:

- a) Increase Fanout limit to reduce buffer replication
- b) Change global Frequency settings to relax the timing requirement
- c) Turn on resource sharing (design specific) to optimize the design

### 40. What kind of Area improvement technique is available in Synplify?

- a) Increase the fanout limit when you set the implementation options. A higher limit means less replicated logic and fewer buffers inserted during synthesis, and a consequently smaller area. In addition, as place-and-route tools typically buffer high fanout nets, there is no need for excessive buffering during synthesis.
- b) Check the Resource Sharing option when you set implementation options. With this option checked, the software shares hardware resources like adders, multipliers, and counters wherever possible, and minimizes area.
- c) For designs with large FSMs, use the gray or sequential encoding styles, because they typically use the smallest area.
- d) If you are mapping into a CPLD and do not meet area requirements, set the default encoding style for FSMs to sequential instead of one hot.

### 41. How do I disable area optimization?

The optimization for timing is often under the expense of area. There is no specific way to disable area optimization. You can improve timing and thereby increase area utilization by using the following options:

- a) Enable retiming option.
- b) Enable Pipelining option.
- c) Use realistic design constraints, about 10 to 15 percent of the real goal.
- d) Select a balanced fanout constraint.

More details on optimization for timing are available in the following document:

[http://www.actel.com/documents/synplify\\_ug.pdf](http://www.actel.com/documents/synplify_ug.pdf)

#### 42. How do I “Disable sequential optimization”?

There is no explicit button or checkbox to disable sequential optimization. This is because there are different types of Sequential Optimizations that are performed by Synplify.

The Synplify Reference Guide [http://www.actel.com/documents/synplify\\_ref\\_ug.pdf](http://www.actel.com/documents/synplify_ref_ug.pdf) gives all the options for disabling optimization.

For example, you can:

- Disable the FSM Compiler.

- Use the `syn_preserve` directive to keep registers in certain cases.

- Open the `Synplify.prj` file in a text editor and use the command

`set_option -no_sequential_opt 1` (Note that the Project Manager overwrites the Synthesis PRJ file every time you invoke synthesis so keep that in mind if choosing this option.)

## TMR Usage

### 43. Which family is TMR supported through Synplify?

It is supported on Actel ProASIC3/E devices as well as Actel's Radiation Tolerant (RT) and Radiation Hardened (RH) devices. You can also get the TMR setting to work for Actel's older Antifuse Device Families. However it is not supported in the commercial AX device family.

Note that in Actel's RTAX device family, better TMR support is available through hardware itself. For Axcelerator RT devices, the Triple Module Redundancy (TMR) is built into the silicon making soft TMR via the Synthesis tool unnecessary for sequential logic.

### 44. Why is TMR macro working in SX, but not in AX family?

There is no software TMR support in Synplify synthesis for the commercial Axcelerator family, but it is available for the SX family. If you are using RTAXS devices, the TMR is built-in (for the sequential flip-flops) in the hardware/device.

### 45. How can I enable TMR for a SX-A device?

For the SX-A device family, in the Synplify Software you need to manually import the file found in the Libero IDE Installation Folder, such as:

```
C:\Actel\\Synplify\synplify_200903A2\lib\actel\tmr.vhd
```

Note that the order of the files in the Synplify project is important and the top level file should be at the very bottom. You can click and hold the top level file in the Synplify project and drag it below the tmr.vhd file.

## Miscellaneous

### **46. Which version of Synplify supports Nano products?**

All versions of Synplify after Synplify 9.6 A.

### **47. Which version of Synplify provides RTAX-DSP support?**

All versions included with Libero IDE v8.6 and later.

### **48. I am having trouble using the HDL Analyst tool.**

The HDL Analyst tool is not available with the regular Synplify tool (synplify.exe). It requires Synplify Pro (shown here: <http://www.actel.com/products/software/libero/synplify.aspx>). Actel currently offers Synplify Pro licenses for free with the Libero Gold 1YR License. However, the default synthesis tool profile in Libero points to the non-Pro synplify.exe. To use the HDL Analyst Tool in Synplify Pro, add a Synthesis Tool Profile which points to the synplify\_pro.exe file in the installation directory.

### **49. How do I create an IP core with the HDL files I have?**

Create an EDIF net-list without IO buffer insertion. This EDIF netlist is sent to the user as an IP. The user must treat this as a black box and include it in his design. User should use the synthesis attribute `fpga_dont_touch` to treat this as a netlist while synthesizing.

Nano devices have only 4 global clock networks. How do I set this constraint?

Use the attribute `/* synthesis syn_global_buffers = 4*/`.

### **50. Why am I not seeing my new port list even after I updated the netlist?**

Although the new port was added in the design, the netlist did not add a buffer to the port since there was no logic in the design which involves the port. Ports not associated with any logic in the design are not shown.

### **51. Why doesn't my multicycle path constraint work?**

The Synplify multi-cycle constraint does not work with a lump of register such as `A[15:0]`. It only works with single register, for example `A[15]`. This problem would occur in the Designer SmartTime constraint editor since you can select multiple registers at the same time using the Actel tools.

Actel recommends you wait to set timing constraints in Designer since there will be optimization done to your design during Designer Compile. The timing data from Designer would be final when compared with the timing data provided by Synplify.

### **52. Why is Synplify not using Global for Set/Reset signals?**

Synplify treats set/reset signals differently from clocks. Synplify global promotion always gives first priority to clock signals, even if some set/reset signals have higher fanout than clock nets. Manually instantiate a `clkbuf` to ensure that the set/reset signal is on a global if you want to use global network for these signals.

### **53. Why does Synplify write out SDC clock constraints even for auto-constraints?**

This is the default behavior in Synplify and cannot be changed. However, you can control the SDC auto-constraints by manually modifying or removing the unwanted constraints.

#### **54. Why is my internal tristate logic not synthesized correctly?**

Actel devices do not support internal Tri-State buffers. If Synplify does not correctly remap internal tristate signals, all internal tri-states must be manually mapped to a MUX.

Actel is the leader in low-power and mixed-signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at <http://www.actel.com> .



**Actel Corporation**

2061 Stierlin Court  
Mountain View, CA  
94043-4655 USA  
**Phone** 650.318.4200  
**Fax** 650.318.4600

**Actel Europe Ltd.**

River Court, Meadows Business Park  
Station Approach, Blackwater  
Camberley Surrey GU17 9AB  
United Kingdom  
**Phone** +44 (0) 1276 609 300  
**Fax** +44 (0) 1276 607 540

**Actel Japan**

EXOS Ebisu Building 4F  
1-24-14 Ebisu Shibuya-ku  
Tokyo 150, Japan  
**Phone** +81.03.3445.7671  
**Fax** +81.03.3445.7668  
<http://jp.actel.com>

**Actel Hong Kong**

Room 2107, China Resources Building  
26 Harbour Road  
Wanchai, Hong Kong  
**Phone** +852 2185 6460  
**Fax** +852 2185 6488  
[www.actel.com.cn](http://www.actel.com.cn)