



ModelSim Simulation Frequently Asked Questions

Version 1.0

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ModelSIM AE vs. ModelSim Full Version (SE/PE)

1. Can I use ModelSim SE/PE with Actel Libero IDE?

Standalone ModelSim does not include Pre-Compiled Actel Libraries and does not set up the compiled library tree in the same manner as the ModelSim Actel tool does.

To use the standalone version of ModelSim with Libero IDE, follow the steps below.

To simulate your design targeting Actel technology, you must have the VITAL or Verilog simulation library. Actel Libero IDE software includes two sets of VITAL and Verilog libraries, the **Source library** and the **Compiled library**.

Source Library

You can install source VITAL and Verilog libraries during Libero IDE installation. After selection, those VITAL and/or Verilog libraries will be installed in the following directory tree:

VITAL Library: <Drive>:/Libero/Designer/lib/vtl/95

Verilog Library: <Drive>:/Libero/Designer/lib/vlog

Full version ModelSim users can compile the Actel library and map it during simulation.

Actel does not recommend installing both ModelSim Actel and a full version of ModelSim on your system.

Compile instructions for VITAL and Verilog libraries in ModelSim for Libero IDE:

ModelSim is integrated with Actel Libero IDE software in such a way that if you run simulation from the Libero IDE Project Manager, it will

- a) Automatically map the compiled VITAL (VHDL) or Verilog library
- b) Compile the source code and testbench

In order to take advantage of this integration, you must compile the VITAL and/or Verilog library in a specific directory. Use the instructions below to specify a target directory.

Vital Library Compile (VHDL)

The procedure below compiles an Actel VITAL library in the

<Drive>:/ModelSim_install/Actel/VHDL directory.

1. Create a directory tree /Actel/Vhdl/src under the ModelSim installation directory. Copy the source library into the src directory.

2. Invoke the ModelSim HDL simulator.

3. Change directory to the <Drive>:/ModelSim_install/Actel/VHDL directory with the command:

```
cd <Drive>:/ModelSim_install/Actel/VHDL
```

4. Create a <vhd_fam> family library directory for your simulator with the command:

```
vlib <vhd_fam>
```

5. Map the Actel VITAL library to the <vhd_fam> directory with the command:

```
vmap <vhd_fam> <Drive>:/ModelSim_install/Actel/VHDL /<vhd_fam>
```

6. Compile the library with the command:

```
vcom -work <vhd_fam> src/<act_fam>.vhd
```

For example, to compile the eX library for your simulator, type the following command:

```
vcom -work ex src/ex.vhd
```

7. (Optional) Compile the migration library. Only perform this step if you are using the migration library. Use the command:

```
vcom -work <vhd_fam> src/<act_fam>_mig.vhd
```

Verilog Library Compile (Verilog)

The procedure below compiles an Actel Verilog library in the <Drive>:/ModelSim_install/Actel/vlog directory.

1. Create a directory tree as /Actel/vlog/src under the ModelSim installation directory. Copy the source library into the src directory.

2. Invoke the ModelSim HDL simulator.

3. Change directory to the <Drive>:/ModelSim_install/Actel/vlog directory with the command:

```
cd <Drive>:/ModelSim_install/Actel/vlog
```

4. Create an <act_fam> family library directory for the simulator.with the command:

```
vlib <act_fam>
```

5. Compile the Actel library with the command:

```
vlog -work <act_fam> src/<act_fam>/*.v
```

6. (Optional) Compile the Migration library. Only perform this step if you are using the migration library. Use the following command:

```
vlog -work <act_fam> src/<act_fam>_mig/*.v
```

Sample script for Pre-Synthesis simulation:

```
# Run this script from simulation directory inside Libero IDE
# where add32.vhd is source code and add32_tb.vhd is testbench
# Libero IDE will not automatically run vsim command and so on
vmap work ./work_presynth
vcom -93 -work work_presyn ../hdl/add32.vhd
vcom -93 -work work_presyn ../stimulus/add32_tb.vhd
vsim work_presyn.testbench
add wave /testbench/*
run 1000ns
```

Sample script for Post-Synthesis simulation:

```
# Run this script from simulation directory inside Libero IDE
# where add32.vhd is source code and add32_tb.vhd is testbench
# Libero IDE will not automatically run vsim command and so on
```

```
vlib work_postsynth
vmap work ./work_postsyn
vcom -93 -work work_postsyn ../designer/add32.vhd
vcom -93 -work work_postsyn ../stimulus/add32_tb.vhd
vsim work_postsyn.testbench
add wave /testbench/*
run 1000ns
```

Sample script for Post-layout simulation:

```
# Run this script from simulation directory inside Libero IDE
# where add32.vhd, add32_tb.vhd and add32.sdf are source code, testbench and
# sdf file
# respectively. add32_0 is the instance for add32 in testbench
# Libero IDE will not automatically run vsim command and so on
vlib work_postlayout
vmap work ./work_postlayout
vcom -93 -work work_postlayout ../designer/add32.vhd
vcom -93 -work work_postlayout ../stimulus/add32_tb.vhd
vsim -sdfmax /add32_0=../designer/add32.sdf work_postlayout.testbench
add wave /testbench/*
run 1000ns
```

Compiled Library

ModelSim Actel Edition users must use pre-compiled Actel libraries for simulation. During installation of Libero IDE series software there is a choice to select a library when installing ModelSim. After selection, those VITAL and/or Verilog library will be installed in the following directory tree:

VITAL Library: <Drive>:/Libero/Model/Actel/VHDL/<fam>

Verilog Library: <Drive>:/Libero/Model/Actel/Vlog/<fam>

Where <fam> are act1, act2, act3, a3200dx, a40mx, a42mx, a54sx, a54sxa, ex, a500k, apa, accelerator, proasic3 and proasic3e.

2. What is the difference between ModelSim AE and other versions of ModelSim (PE/SE etc.)?

ModelSim AE is functionally equivalent to ModelSim PE/SE. However, simulations may run slightly slower when compared with SE/PE.

Some of the other limitations of ModelSim AE as compared to SE/PE are:

- Supported Operating System: Windows
- Advanced Optimizations : Not supported
- Performance Analyzer : Not supported
- C debugger : Not supported
- Dataflow window : Not supported
- Waveform Comparison: Not supported

- Code Coverage: Not supported
- Standalone Viewer: Not Supported
- System C: Not supported
- Assertions(PSL): Not supported

Comparison between various ModelSim full versions:

http://www.mentor.com/products/fv/modelsim/upload/ModelSimDE_Compare.pdf

3. Does ModelSim AE support the code coverage feature?

No. Code Coverage is a licensed option for ModelSim PE/SE. You would need to purchase a license to be able to use this feature.

Once you have a license, you need to set the code coverage option for the compile, and then load the design with coverage enabled, and then the menus are enabled. The code coverage chapter of the ModelSim User's Manual includes all the relevant information.

4. ModelSim does not support the waveform save and comparison function. Is this true?

You are correct; ModelSim AE does not support Waveform Save and Comparison. You need ModelSim SE. In the Actel Edition you can only export a Bitmap (BMP) Image of the waveform.

5. Is there a way to force the primitive to not go X's in the simulation? In some silicon libraries a "nox" notifier can be used? Is there something similar?

Our libraries are not set up to support the nox notifier. We do not have any way for you to do this in your simulation, if you have X Values coming from a module, then we suggest that you initialize the module.

Alternatively, you can use the "force" command.

Example: `force signal_name 0 0, 1 200`

It will set the signal to '0' at 0 ns and to 1 after 200 ns.

Library Issues

6. Where can I find the ModelSim simulation library for standalone users?

For Libero IDE v8.3 and above, the precompiled libraries are found in the folder

```
<Libero83_install>\Designer\lib\modelsim\precompiled
```

And un-compiled libraries are under the folder

```
<Libero83_install>\Designer\lib\vt1\95
```

And for versions prior to v8.3, these files can be found under (using D:\Libero80 as the installation directory).

```
D:\Libero80\Designer\lib\vt1\95
```

```
D:\Libero80\Designer\lib\actel (VHDL or verilog)
```

7. Do I need to add the specific family library statement into the VHDL source code for functional simulation?

If you have instantiated any Actel primitives in your VHDL source code, like HCLKBUF, then you need to add the specific family library statement in the source code for functional simulation. For example:

```
library ieee;
use ieee.std_logic_1164.all;
library a54SXA; ----if your target device is a54SXA
entity Top is
...

```

8. When using ModelSim Standalone as part of the Libero IDE flow, the following errors appear:

```
# -- Loading package standard
# -- Loading package std_logic_1164
# ** Error: (vcom-13) Recompile
```

You need to Refresh the syncad_vhdl_lib library.

9. How can an older version of ModelSim be used with a newer version of Libero IDE or vice versa?

Whenever you use ModelSim versions which differ by a number instead of only a letter, you will need to recompile libraries. For example, ModelSim 6.3e and 6.3f can use the same precompiled libraries. However, if you move to ModelSim v6.4a then you need to recompile the libraries.

10. ** Fatal: (vsim-3381) obsolete library format for design unit.

To prevent this error, right-click the relevant library in ModelSim and choose the refresh option.

Re-compile the libraries if required.

11. Does ACTEL support ProASIC3 libraries for the Eagle EDA tool?

We do not support EAGLE EDA.

12. The simulation file (proasic3.v) includes the register "NOTIFY_REG". Is there any way to use this register? Also, if +notimingchecks switch with vsim is used in ModelSim, it will disable all timing checks. So, can we mask some timing violations but not all?

notify_reg cannot be user-controlled. It is an optional register which does not change the behavior of the timing check.

This register is used to model the module behavior in the event of violations like setup/hold etc.

There is no way to disable selected timing checks. Even if you change the value of that register, it will not disable the timing check.

13. When running Libero IDE on Solaris or Linux, simulating the design using ModelSim results in an error.

```
# ** Error: (vsim-13)
Recompile /net/intsun03/export/home1/test_area/ModelSim_sol/modeltech/actel/vhdl/ex.inbuf(vital_act) because
/net/intsun03/export/home1/test_area/ModelSim_sol/modeltech/sunos5acoem/./iee
e.vital_primitives has changed.
```

The technology libraries that are used for simulation are precompiled and need to be refreshed.

In ModelSim, go to the Library tab, right-click the technology library and choose refresh.

License Issues

14. How do I get a new Free Libero IDE Gold 1Year License?

Go to the website: <https://www.actel.com/portal/default.aspx?r=1>

Enter your Customer Portal Login. If you don't have a Portal Login, create a new profile.

Once you login, click **Request a Free License**.

Select the Libero IDE Gold Node Locked License for Windows

Enter the Volume ID (DISK ID of the C: Drive)

Click **Submit**.

You will receive your new license file via the email address associated with your Web Portal Profile with installation instructions.

Please follow the License Install Instructions carefully.

15. # ACTEL version supports only a single HDL # ** Error: (vsim-3039) / Why doesn't a mixed HDL simulation run?

Check your license. Your license should have both vhdl and verilog feature lines, which means that you should be able to run mixed language simulation. See the document below for more information.

http://www.actel.com/documents/modelsim_tutorial_ug.pdf

If your license is correct:

You might have not installed both vhdl and verilog libraries. Please check your installation. For example if you go to installation directory

```
<Libero IDE install directory>\Designer\lib\modelsim\precompiled
```

You should see both verilog and vhdl folders. If so, then you have installed both verilog and vhdl library models.

16. ModelSim license parallel port dongle: I had Libero IDE v8.0 and just upgraded to v8.3 but now ModelSim is no longer working; it throws a license checkout error message.

You need to install the updated driver from

<http://www.actel.com/products/software/libero/drivers.aspx#par>

17. Fatal License Error: Evaluation Error Code: 105

Check C:\Windows or, C:\Windows\system32 folder for two files called "mti_enc" and "mti_enc2" (be sure to set your folder options to view hidden files/folder).

If they are there REMOVE THEM then try ModelSim again.

18. ModelSim License Error# ** Error: Failure to obtain a VHDL simulation license.

You may have merged another license with your Libero IDE license, specifically one with server feature lines. Keep these licenses separate and this will fix the problem.

The system clock has been set to a future date (system has files with future dates).

19. I installed Actel Libero IDE. I am able to open the Libero IDE Project Manager but cannot open ModelSim. It is not giving any warning or error. But if I click ModelSim from the Project Manager, it shows the ModelSim icon and then does not open anything.

Redundant ModelSim license causes this issue.

Example:

```
MGLS_LICENSE_FILE=27008@10.100.33.206;27008@10.100.33.203;27008@10.100.33.205;  
C:\flexlm\License.dat;
```

Please do a search in all drives of your pc for "license.dat" and see whether it resides only in C:\flexlm\license.dat

If you see this file is also somewhere else then you need to delete the duplicate.

Also, if you have license file for the full version ModelSim, you need to delete it.

ModelSim Features

20. How do I set the simulation run time manually?

Libero IDE automatically sets the simulation run time to 1000ns. How do I set the time in ModelSim so it runs 6ns?

- a) In **Project Manager**, right-click the **ModelSim** icon and choose **Options**
- b) Change the simulation runtime and click **OK**. The automatically generated run.do will reflect your selected runtime.

21. How do I turn off warnings in ModelSim?

In ModelSim

1. Select Simulate – Runtime Options
2. Select the **Assertions** tab and enable the **Warning** field

22. How can I turn off the ModelSim vital glitch warning during the post-layout simulation?

Use the +no_glitch_msg flag for the vsim command. Though it is not always recommended, it is useful to look at the real problem (setup or hold)

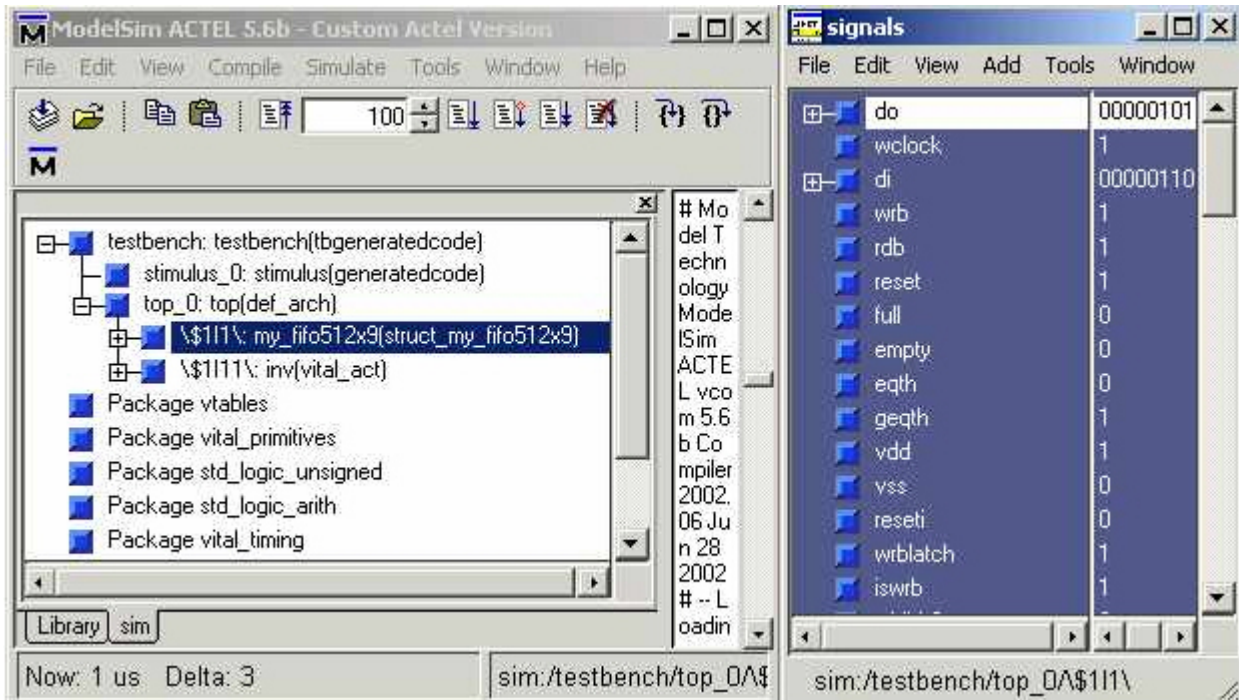
Example:

```
vsim +no_glitch_msg -L apa -L postlayout -t lps -sdfmax  
/berkana_0=D:/FA/project_dir/TestVector/designer/impl1/berkana_ba.sdf  
postlayout.testbench
```

23. How can I view the sub module signals in the ModelSim wave window?

You can add sub module signals by browsing through the hierarchy and selecting the sub module from the ModelSim command window, then select ViewSignals from ModelSim pull down menu.

Inside the Signal window, you can highlight signals you want to add in the Wave window, then click AddWaveSelected Signals or use AddWaveSignals in Region to add all signals related to this sub module (as shown in the figure below).



Restart the simulation and run it again. If you want to save the wave format you have added into the wave window, use the command Save Format inside the Wave window.

24. How can I retain my radix in the wave window after I manually change them to a desired value for all simulations in a particular project?

If you want just certain signals to have a different radix, then you need to set these manually and use the Save format menu to save these values to a wave.do file that you can then execute with the do wave.do command.

In the Libero IDE environment you need to change a line in the run.do file (include do wave.do command in the script) and save run.do as run1.do. In **Project > Settings > Simulation** use this run1.do instead of the default run.do.

25. How can we group a bus for viewing a simulation result?

Here is an example of grouping a signal in a run.do file:

```
virtual signal { sim:/testbench/top_0/u1/\count[15] /Q &
                sim:/testbench/top_0/u1/\count[14] /Q &
                sim:/testbench/top_0/u1/\count[13] /Q &
                sim:/testbench/top_0/u1/\count[12] /Q &
                sim:/testbench/top_0/u1/\count[11] /Q &
                sim:/testbench/top_0/u1/\count[10] /Q &
                sim:/testbench/top_0/u1/\count[9] /Q &
                sim:/testbench/top_0/u1/\count[8] /Q &
                sim:/testbench/top_0/u1/\count[7] /Q &
                sim:/testbench/top_0/u1/\count[6] /Q &
                sim:/testbench/top_0/u1/\count[5] /Q &
                sim:/testbench/top_0/u1/\count[4] /Q &
                sim:/testbench/top_0/u1/\count[3] /Q &
                sim:/testbench/top_0/u1/\count[2] /Q &
                sim:/testbench/top_0/u1/\count[1] /Q &
                sim:/testbench/top_0/u1/\count[0] /Q } count_vector

add wave -nouupdate -format Literal -radix decimal
/testbench/top_0/u1/count_vector
```

26. How do I simulate with multiple SDF files?

To simulate with multiple SDF files, you can modify your run.do file:

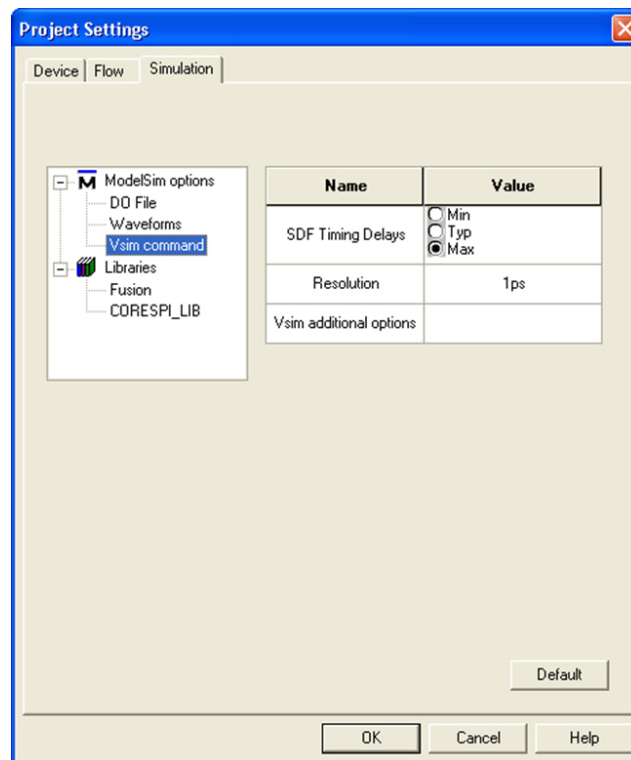
```
vsim -L fusion -L postlayout -t lps -sdfmax /Project_Dir/File1.sdf -sdfmax
/Project_Dir/File2.sdf -sdfmax /Project_Dir/File3.sdf postlayout.testbench
```

Make sure that each SDF file corresponds to a specific top-level module in your netlists.

27. ModelSim runs the simulation for the worst case temperature value. How can we simulate our design for both the best case and the worst case temperature values on ModelSim?

Set it in the Libero IDE Project Manager before running the simulation in ModelSim.

Set this option in the Project Manager Project Settings. Review the SDF timing delays. You can choose Max (worst case), Typ (nominal) and Min (best case) , as shown in the figure below:



28. Is it possible to simulate the JTAG interface within ModelSim?

Yes, it is possible to simulate the JTAG interface, if UJTAG macro has been instantiated in the design. In which case, the simulation emulates some functionality of the JTAG interface as seen from the FPGA chip. Check the simulation library file (search for UJTAG):

```
~Designer/lib/actel/vlog/igloo.v
```

Post-Synthesis vs. Pre-Synthesis Simulation (Mismatch/Errors)

29. My post-synthesis simulation is different than my pre-synthesis simulation. Why?

Review the synthesis log. In some cases, your RTL code has some initialization or functions that are not used and may be removed during synthesis.

Please review and see if the log contains any suspicious info.

30. Pre synthesis simulation runs but post synthesis simulation displays all outputs in red. Why?

Check the Reset signal.

You may not have power on reset on the internal registers.

You need to apply reset. If it is floating, it will cause the module to initialize to unknown and then it is unknown forever.

This does not happen in silicon. In silicon, it will be in a specific state (most likely all zeros).

So, you can either:

- Apply reset signal and change the code.
- Force the FFs/Registers to reset by using ModelSim force command.

31. ****Error: (vsim-3170) Count not find "<Project_Dir>\simulation\presynth.testbench'** **Error loading design**

ModelSim Simulation options have not been set properly (**Project Settings > ModelSim > Options**)

Make the following changes:

Right-click the Simulation tab in the Project Flow window or select **Project > Settings > Simulation**

Testbench module name: specify your testbench module name

Top level instance name in the testbench: instance name of the DUT

Please see the screenshot below for an example.

32. **#error: (vsim-23)unable to change to directory path "postsynth.test"** **#No such file or directory.(errno=ENOENT)**

ModelSim Simulation options have not been set properly (**Project Settings > ModelSim > Options**)

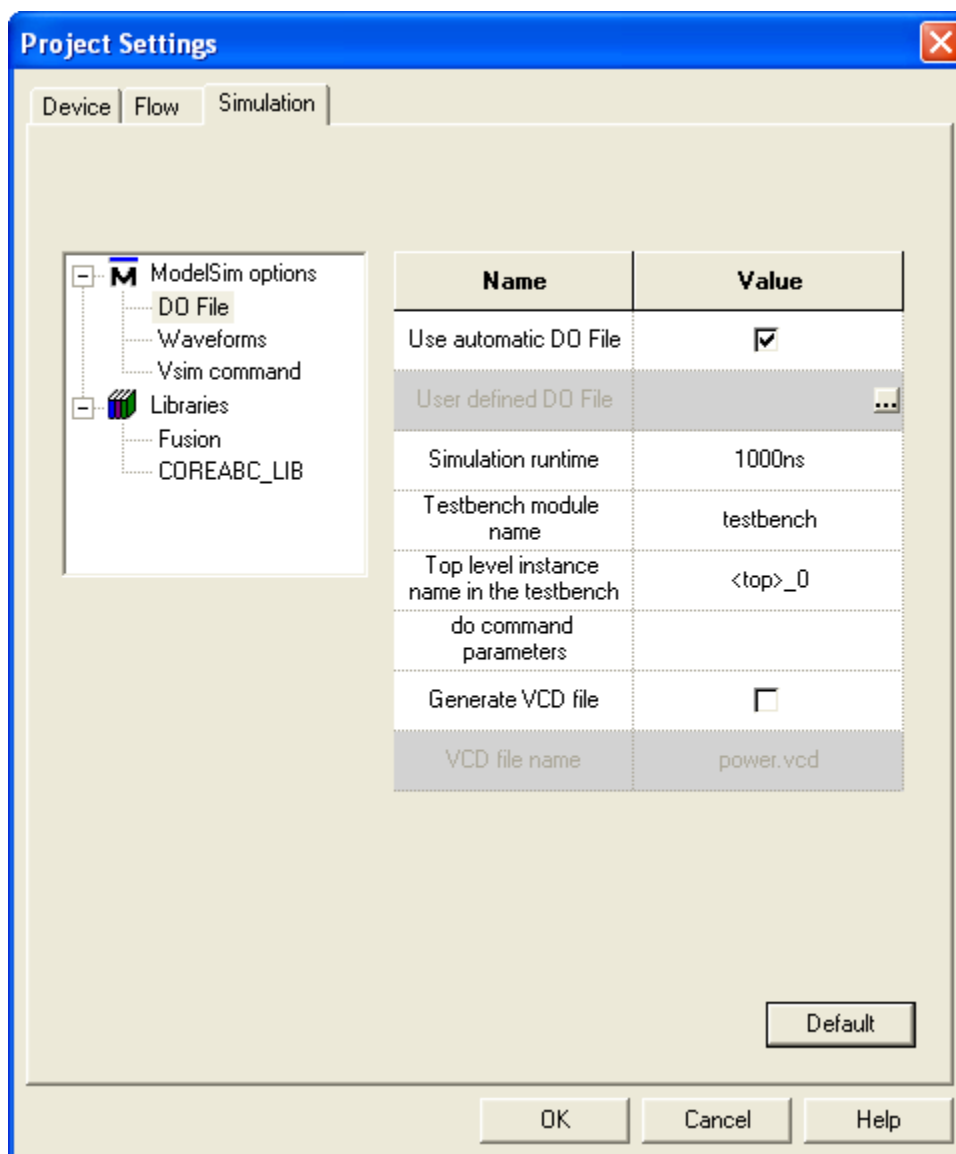
Make the following changes:

Right-click the Simulation tab in the Project Flow window or select **Project > Settings > Simulation**

Testbench module name: specify your testbench module name

Top level instance name in the testbench: instance name of the DUT

Please see the screenshot below for an example.



Post-Layout Simulation Errors

33. Why does the simulation show no violation of setup and hold times, but the simulator returns a warning?

This issue is caused by incorrect interpretation of the delays.

You may be viewing the signals at the internal input ports of the macro. You must add the signal *_ipd to your simulation waveform window.

For details please refer to: <http://www.actel.com/kb/article.aspx?id=KI44946>

34. Why there is a difference between the results of the static timing analysis in Designer and post-layout simulation with ModelSim?

This issue is caused by incorrect interpretation of the delays.

You may be viewing the signals at the internal input ports of the macro. You must add the signal *_ipd to your simulation waveform window.

For details please refer to: <http://www.actel.com/kb/article.aspx?id=KI44946>

35. Timing Violation errors or warnings during post layout simulation.

For example, take the error message:

```
# ** Error:
C:/Actel/Libero_v8.5/Model/win32acoem/../../Designer/lib/modelsim/precompiled/
vlog/src/54sxa.v(8363): $setup( posedge D:30272700 ps, posedge CLK &&&
Enable1:30273400 ps, 900 ps );
# Time: 30273400 ps Iteration: 1 Instance: /testbench/NJFPGA_0/\$1I255
/\$1I227
```

The Error Messages contained in the ModelSim Simulation Error Log is actually timing violation errors notifying you about timing violations in a post-layout Back Annotated Timing Simulation with respect to the setup, hold, and pulse width restrictions specified in the device library and in the SDF Timing Delay file for the design under test. You must evaluate each message and determine if there is a legitimate timing issue with the design that will cause the design not to function or whether you can ignore certain errors.

The example error says that Instance /testbench/NJFPGA_0/\\$1I255 /\\$1I227 of the design shows a setup time violation on the positive edge of a flip-flop. It shows that the minimum setup time on the D port is 900ps, but from the simulation, only 700ps setup time is used (posedge of D at 30272700ps while posedge of CLK comes at 30273400ps). These checks are coded into the device library source file and the delays for the specific instances of the design are in the SDF file.

Also, these messages may appear if you are missing the timescale definition in the testbench but have defined in design files..

Known Issues

36. When I run ModelSim, my computer hangs, with "vsimk.exe" at 100% CPU usage. I cannot shut down ModelSim during this time. I must wait about 10 minutes until vsimk.exe stops running. Why?

This is a known issue with the co-existence of two versions of ModelSim (non Actel versions). Please uninstall one.

Mentor tools conflict with each other if same tool is installed twice.

You need to uninstall one of them. If you want to keep ModelSim that is not part of Libero IDE then in Libero IDE tools profile link it (link the modelsim.exe file location).

37. In PLL simulation (pre-synth, post-synth and post route) some output frequencies do not show up as expected.

This issue is for simulation only. The silicon does not have this problem.

This is caused by round-off in the PLL simulation model. For example, a PLL is generated with 25MHz input and 300 MHz and 100 MHz output. 25 MHz clock has a period of 40000 ps. In order to generate both 300MHz and 100MHz output clock, the input clock period is first divided by 12 (to generate the 300MHz clock) and then multiplied by 3 (for the 100MHz clock). When 40000 ps is divided by 12, the result is 3333.333 ps. The model rounds this up to 3334 ps. When 3334 ps is then multiplied by 3, the result is 10002 ps. This causes the 100MHz (and 300MHz) clocks to appear to drift relative to the 25MHz input clock.

38. Post-synthesis and post-layout simulation gives invalid results for the INOUT bus. INOUT bus with initial value 'U' Within Netlist Causes Unknown In Post-Synthesis and Post-Layout Simulation. How do I get a valid result?

1. If speed is not a critical design issue, then turn off Cross-Boundary Optimization in Synplify by using the `syn_hier=hard` attribute in Synplicity to stop reconstruction of the hierarchy block, and to stop generating the INOUT bus. The corresponding HDL netlist generated by Designer results in correct simulation.

2. If Cross-Boundary Optimization is required to improve performance, post-synthesis and post-layout HDL netlists need manual modification. Add initial value 'Z's to the INOUT bus at the Entity port declaration. For example:

```
Entity Remove_Unknown is
```

```
Port (A: in std_logic;
```

```
B: in std_logic;
```

```
INOUT_BUS: inout std_logic_vector (7 downto 0) := (others => 'Z'); - - <- Add initial value 'Z' here
```

```
C: out std_logic);
```

```
End Remove_Unknown;
```

After this modification, post-synthesis and post-layout simulation gives valid results for the INOUT bus.

For further details, please refer to the link below:

<http://www.actel.com/kb/article.aspx?id=KI40672/41006>

39. SmartPower does not annotate all pins when the VCD file generated by ModelSim is imported into Designer.

Close to 100% annotation can only be expected if you are importing a post-layout VCD. If you import pre-synthesis and post-synthesis VCD's, the SmartPower netlist may be different from the netlist that was simulated.

Remove all Escaped characters in the VCD file manually. For example, if you have the following in your VCD file:

```
$var wire 1 - \cnt_c[0]\ $end
```

```
$var wire 1 . \cnt_c[1]\ $end
```

```
$var wire 1 / \cnt_c[2]\ $end
```

```
$var wire 1 0 \cnt_c[3]\ $end
```

Modify the signal as shown below:

```
$var wire 1 - cnt_c[0] $end
```

```
$var wire 1 . cnt_c[1] $end
```

```
$var wire 1 / cnt_c[2] $end
```

```
$var wire 1 0 cnt_c[3] $end
```

Re-import the modified VCD file into Designer.

Please refer the following document for more details: <http://www.actel.com/kb/article.aspx?id=KI26109>

Miscellaneous

40. ModelSim Simulation Error #**Fatal:(vsim-3881)

Check the vsim command line to insure that the correct testbench is targeted

41. How do I simulate two Actel FPGAs together in a system simulation?

Libero IDE cannot handle multiple designs at once, but ModelSim can. Create a top level netlist with the two devices. Then modify the inputs/outputs in the SDFs to take into account the delays between the two devices. Run ModelSim, simulate the new top level, but load the SDFs for each device. (It is possible to specify a SDF for an instance within a design, please refer to the ModelSim User's Guide at http://www.actel.com/documents/oem_man.pdf.)

42. Failed to find instance

ERROR: C:/Designs/annotations/interface.sdf(15): Failed to find INSTANCE '/testbench/ramwrn_1'

ERROR: C:/Designs/annotations/interface.sdf(24): Failed to find INSTANCE '/testbench/block_1'

The problem is that the INSTANCE hierarchical path that is mentioned does not exist in the design that is loaded. By default, the hierarchical path that is used is the top-level entity (testbench) concatenated with the instance path that exists in the SDF file (ramwrn_1). The top-level entity is thus considered the "region", the level of hierarchy that is applied to the SDF file. This default region is used if no specific region is supplied. Excerpt from C:/Designs/annotations/interface.sdf file

```
(CELL
(CELLTYPE "BUF")
(INSTANCE ramwrn_1) // SDF file instance path
(DELAY
(ABSOLUTE
(IOPATH IO O (20:20:20) (20:20:20) )
)
)
)
```

Typically, an SDF file is written without the knowledge of a top-level testbench in the design hierarchy and therefore the default path is incorrect. This is a very common situation. There are other situations where you are only annotating data to a portion of the design and you need to specify the level of the hierarchy that is applied to the SDF file.

In the example, the correct "region" is the testbench entity name (testbench) and then the instantiation name of the design (dut) in the testbench architecture, not the design's entity name. Therefore, the region would be "/testbench/dut".

To specify the "region" in ModelSim:

From ModelSim choose **Load Design > SDF Tab > Add > Apply to Region**

From the command line type: `-sdftyp <region>=<SDF file path/name>`

Command line for this example

```
vsim -sdftyp /testbench/dut=./annotations/interface.sdf testbench
```

Note: This example uses the C:/Designs directory. The INSTANCE hierarchical path would now be /testbench/dut/ramwrn_1, which is a valid path in the design, and not the default /testbench/ramwrn_1.

If the default path does not work you must ensure that the region concatenated with the instance path in the SDF file results in a valid hierarchical path that exists in the loaded design.

43. # Error: couldn't open socket: invalid argument Trouble making server

Check Firewall, Anti-Spyware, and Anti-Virus settings to make sure 'vish.exe' and 'vsimk.exe' are allowed to run.

44. ** Error: (vsim-3174) Package 'D:\Actel\Libero_v8.4\Model\std.standard' requires a body.

If you get this message for the standard package, this package has been corrupted and you need to uninstall and reinstall ModelSim.

To do so, from the Start menu choose **All Programs > Actel Libero IDE vx.x > Uninstall and Modify Libero IDE**.

Then follow the instructions in Installshield to repair the ModelSim installation.

45. I cannot get the input waveforms that I defined in Waveformer Lite to match the input waveforms that are shown in ModelSim when I run simulation. Why?

This is a limitation with Waveformer Lite (WFL). No matter what radix you used for your data, the tool takes it as HEX and therefore you are seeing the 6 least significant binary bits of your data entered as HEX in ModelSim.

46. Why are the backannotated timing results different than what I can see in SmartTime?

Please check the TIMESCALE defined at the top of SDF file (usually set as TIMESCALE 100ps). This would mean that 100 unit delay would actually mean a 10 ns delay.

47. In Libero IDE Project Manager Settings there is a way to send extra command line arguments to the VSIM command. Is there a way to add a command line argument to the vlog command?

No, you cannot use the Project Manager GUI to add an argument to the vlog command.

You can modify the run.do script that Libero IDE automatically generates and add your extra command line arguments to the vlog command in the run.do script.

In your Libero IDE Project Simulation folder, there will be an auto-generated run.do script (if you have invoked any simulations from within Libero IDE Project Manager). You can modify this run.do script to add your extra vlog arguments. Note that the Project Manager automatically generates the appropriate run.do script depending on whether a pre-synthesis, post-synthesis, or post-layout simulation is being run (since the source files will differ).

If you want to take manual control over this scripting process, after running each type of simulation, save a copy of the run_.do script in your project's simulation folder making sure you name it appropriately (i.e. run_presyn.do). Then, once you have an example of the run.do scripts for each type of simulation, you modify the scripts as needed, and then disable the automatic run.do script creation in Project Manager and manually specify which script should be used before each simulation using the **Project > Settings > Simulation** tab. You can find the vlog arguments listed in the ModelSim command reference at http://www.actel.com/documents/ModelSim_cmd_ref_ug.pdf

Useful Links

Complete instruction on how to run standalone ModelSim

<http://www.actel.com/kb/article.aspx?id=SL1123>

http://www.actel.com/documents/ModelSim_Compil_Ins.pdf

Writing an Analog TestBench

http://www.actel.com/documents/analog_testbench_UG.pdf

Miscellaneous Links:

<http://www.actel.com/products/software/libero/modelsim.aspx>

http://www.mentor.com/products/fv/modelsim/upload/ModelSimDE_Compare.pdf

http://www.actel.com/documents/modelsim_tutorial_ug.pdf

http://www.actel.com/documents/modelsim_ug.pdf

http://www.actel.com/documents/modelsim_cmd_ref_ug.pdf

http://www.actel.com/documents/WaveFormerLite_ug.pdf

http://www.actel.com/documents/TimingDiagramEditors_ug.pdf

<http://www.actel.com/products/software/libero/licensing.aspx>

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