Can anything

Dwindling numbers of design starts mean the future of ASICs is not looking too rosy. Dick Selwood investigates

According to Gartner, worldwide ASIC design starts have plummeted from a peak of over 11,000 starts in 1997 to fewer than 4000 in 2005. At the same time, FPGA design starts are currently running at over 90,000 a year and rising. Does this mean that the ASIC is on its way out? Is it being squeezed out by the rising costs of design tools, the complexities of design, the cost of using leading edge fabs and the millions of dollars for mask sets at the top end and by increasingly larger and more capable FPGAs at the bottom?

In some cases it depends on what you mean by an ASIC. Dennis Kish, of FPGA maker Actel, looks at ASICs as one way for mass customisation to meet a specific need in the market – providing the user with exactly what they want in functionality, at the right price, right performance and right power.

> **"One very important area is analogue/mixed signal"**

Leading edge

Traditionally 'right' performance and power has meant the 'best' performance and power, achieved by using the leading edge in process technology, and requiring the latest (and most expensive) design tools. For these products design costs alone can be between $20 and $50 million, according to veteran journalist, Ron Wilson, who chaired a Silicon Valley panel on this topic last month. In order to cover these costs, plus the mask sets and processing charges, a very high volume market has to exist, and even then unit costs can be high.

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Vince Hopkin, of ASIC vendor AMI, says that all ASICs are not alike. There is, indeed, a role for ASICs that are made using the latest process technology, but not every application needs to push power, performance and capacity to the limit. For these applications 90nm technology, or finer, is not needed: instead the proven technologies of 130nm, or even 0.5 micron may provide appropriate technology, with lower tool and design costs, and lower mask costs. Hopkin argues that mid-range technologies can address as large a proportion as 60% of potential applications.

He also argues that with this approach there is a far higher chance that a design will also turn into a real product, unlike 10 years ago when less than 50% of design starts went into production. With high success and relatively low cost, the risk is reduced to the point where it is viable for a start-up to use an ASIC.

Of course many start-ups will not take that risk and will start with an FPGA, at least for proof of concept if not for production. Kish is, not surprisingly, confident that FPGAs are a genuine production option. Now that they are cheap and fast, with acceptable power, they provide the new route to mass customisation. Unlike the EDA tools for an ASIC or full custom chip, FPGA design tools are low cost: Actel, like the other FPGA companies, has around half its development effort in software and sees supplying the tool chain as part of the product they offer – just as microcontroller manufacturers also supply reasonably priced development tools.

Greater logic

Wilson points out that the total logic in today's 4000 ASIC starts is greater than that in the 11,000 starts ten years ago, with a significant proportion of the designs encompassing functions that would previously have been spread across three or four chips. In his view, ASICs are transitioning from a few islands of IP in a sea of RTL, to lots of IP, often very large blocks, stitched together with RTL. This is analogous to printed circuit boards where chips of specific functions, such as processors, I/O or memory were linked with glue logic.

Extending this is the platform approach, where a manufacturer offers a device aimed at a specific application, such as automotive or set-top boxes. The design is not complete, but includes large blocks of IP, such as processors and special buses like CAN for automotive etc. The IP may be configurable, to a greater or lesser degree, allowing the platform to be tailored in manufacturing to meet the OEM's specification and provide market differentiation. Once out of the fab, the design is normally locked, but there have been attempts to add field programmable logic for greater flexibility. Wilson points out that while platforms may be considered as a configurable version of ASSPs, they are clearly a lower cost option compared to ASICs.

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Verified?

Returning to ASICs, the approach of using large elements of IP linked with some RTL resources brings its own problems. While the analogy with a circuit board works at one level, Wilson points out that reality is much more complex. Chips on a board have a limited number of pins and effectively a limited number of states. IP can have many interfaces and many states, so chip design, and particularly verification, continues to be a complex issue. Hopkin adds that, at the moment, there are still problems with IP quality and much third party IP is not well designed and more is not proven. He feels that, for success, IP has to be not just qualified as a prototype in a process, but also proven in production. Even then it can take multiple implementations before all the

Key Points

- ASIC design starts have fallen from 11,000 in 1997 to fewer than 4000 in 2005
- FPGA design starts are currently running at 90,000 a year and rising
- Not every application needs to push power, performance and capacity to the limit. ASICs in these applications can use older process technologies resulting in lower costs
- FPGAs are now cheap and fast and are providing a new route to mass customisation
- Unlike the EDA tools for an ASIC or full custom chip, FPGA design tools are low cost, as supplying the tool chain is seen as part of the product by the vendor
- The total logic in 2005's 4000 ASIC design starts is greater than the logic in the 11,000 design starts ten years ago, with a significant proportion of designs encompassing functions that would once have been spread across three or four chips
- One view is that ASICs are transitioning from a few islands of IP in a sea of RTL, to lots of very large IP blocks stitched together with RTL
- The platform approach has also risen as a lower cost option than ASICs
- One reason for choosing an ASIC is security: hard-earned knowledge is intrinsically safer in an ASIC

save the ASIC?

bugs are found, even in something as simple as a PLL circuit. Previous implementations are even more necessary for IP aimed at military and aerospace applications and in automotive applications, where temperature range qualification is essential. Hopkin is also cautious about design verification: while it is not sufficient to treat the IP as a black box for verification, third party IP often doesn't come with enough data to be integrated well into the verification elements of the design flow.

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If the ASIC is under pressure from platforms at the top end, a similar process in FPGAs is pushing from below. FPGA vendors are also providing large, pre-designed structures, such as processors (in Actel's case, industry standard ARM cores), memory, I/O and communication functions such as PCI-Express, in addition to a wide range of smaller IP elements. The larger structures may be, in some cases, configurable and, by definition, the remaining logic is field programmable, providing a much greater degree of flexibility.

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Retargeting

This flexibility is what makes an FPGA such a good choice for developing early versions of products, before converting to an ASIC or a structured ASIC for volume production. Hopkin argues that the ASIC, and the structured ASIC in particular, has a significant role in retargeted FPGAs, providing power and unit cost savings. Another reason for choosing an ASIC is security, he suggests: the hard-earned knowledge that goes into a device is intrinsically safer in an ASIC than in an FPGA where configuration data needs to be reloaded on power-up and the data stream can be monitored and copied. This insecurity also makes an FPGA unsuitable for many defence applications (Kish would argue that flash and anti-fuse FPGAs do not have this problem and are intrinsically secure).

So far discussion has centred on digital circuits, but increasingly there are other needs as integration pushes more functionality onto a single device. One very important area is analogue/mixed signal. Both Kish and Hopkin emphasise the growing importance of analogue/mixed signal elements in designs, and both work for companies that provide products to meet this requirement: Actel now has an FPGA family with analogue blocks, and AMI has plans for further analogue developments.

Evolution

The conclusion is that the ASIC is not in need of saving, it is just evolving. There will still be applications that need to push the performance and capacity limits, and the traditional ASIC approach will continue to provide the resource needed. These will be joined by more application targeted platform devices with large, configurable structures, supplied as IP, linked by configurable glue logic, with configuration taking place in the fab. FPGAs will be mounting a similar approach, with customisation through programmability and tools replacing configuration by mask sets. In the middle will be an area using conservative technologies, proven tools and proven IP that will address traditional ASIC concerns of right price, right performance and right power. ■