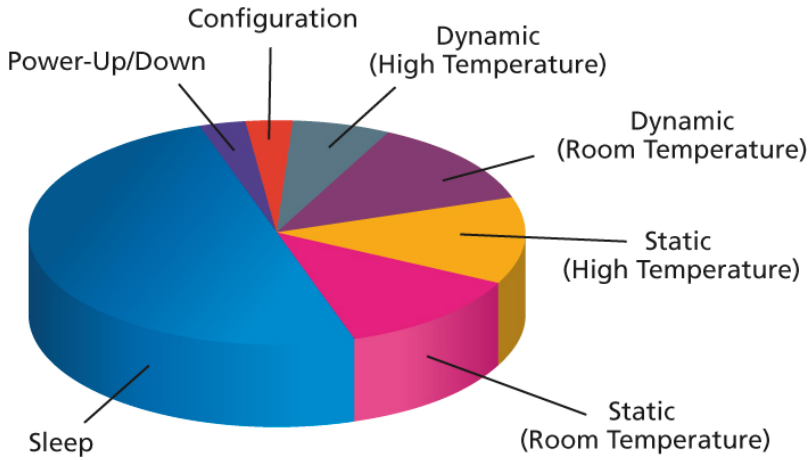
Total System Power in FPGAs

FPGA Power

- Unlike any other semiconductor devices, FPGAs have unique power characteristics
- There are several components to power in FPGAs
  - **Power-Up**
    - **Inrush power**
    - **Configuration power**
  - **Operation (over temperature)**
    - **Static**
    - **Dynamic**
    - **Sleep**
  - **Shutdown**



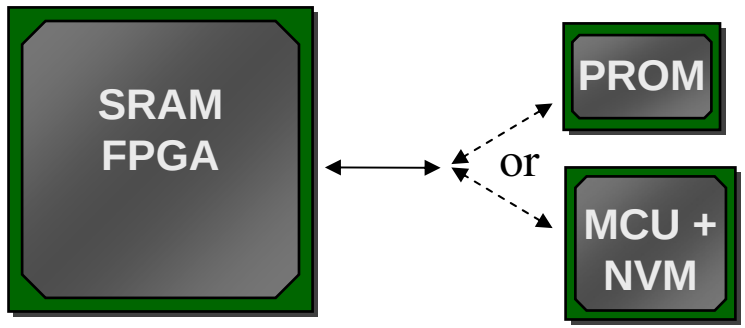
System Power Profile (over time) – Example

FPGA Power Characteristics

- The power profile of FPGA devices varies depending on the underlying technology used to create the programming element
  - **SRAM FPGAs, SRAM Hybrid FPGAs, Flash FPGAs, Antifuse FPGAs**
- SRAM-based FPGAs have all 4 significant power components
  - **Inrush, configuration, static, dynamic**
- Flash and antifuse FPGAs (like ASICs) have only 2 significant power components
  - **Static and dynamic**

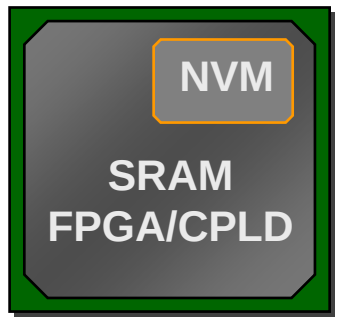
SRAM

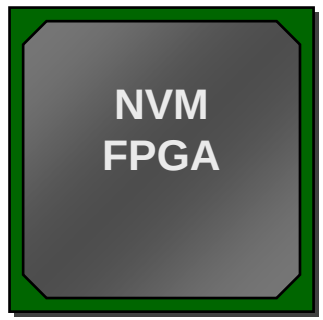
SRAM FPGA with boot



SRAM

Hybrid FPGAs/CPLDs – SRAM fabric Loaded from nonvolatile memory (NVM) on-chip





NVM

True Flash and antifuse FPGAs

System Power
Power-up

Power-Up
Inrush Current

- The power spike caused when a system is powered up and the logic states are not determined
  - **SRAM FPGA – Core cell logic is in contention because the volatile SRAM is indeterminate at power-on**
    - **SRAM FPGA can consume > 1 Amp at power-up**
  - **SRAM FPGA – Requires power sequencing to mitigate the problem**
- Power system must be sized to accommodate for the inrush
  - **Not providing enough power can prevent the system from properly powering up**
  - **Extra sequencing device adds design overhead and cost**
- Flash and antifuse FPGAs have minimal inrush similar to that of an ASIC

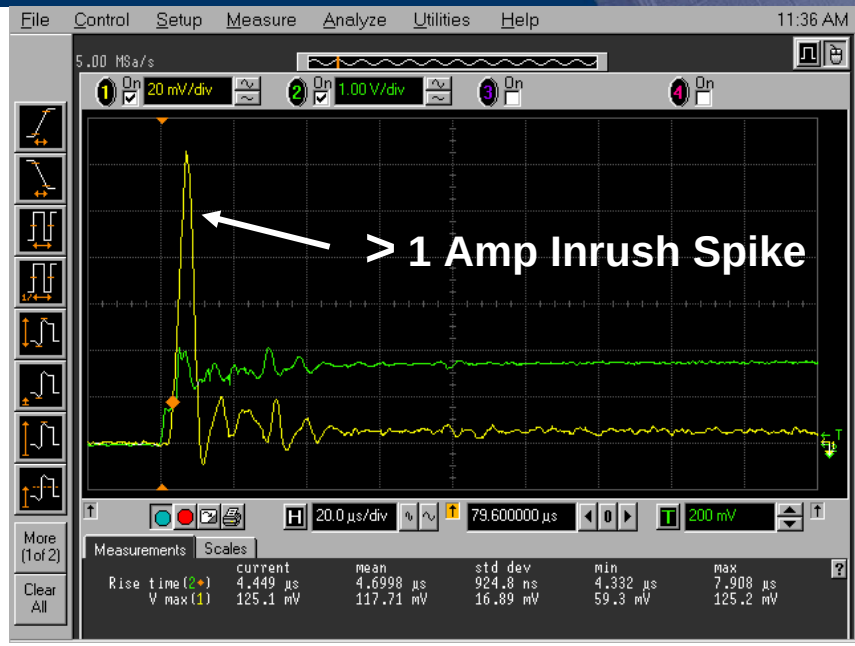
Inrush Current Spike SRAM and NVM FPGAs

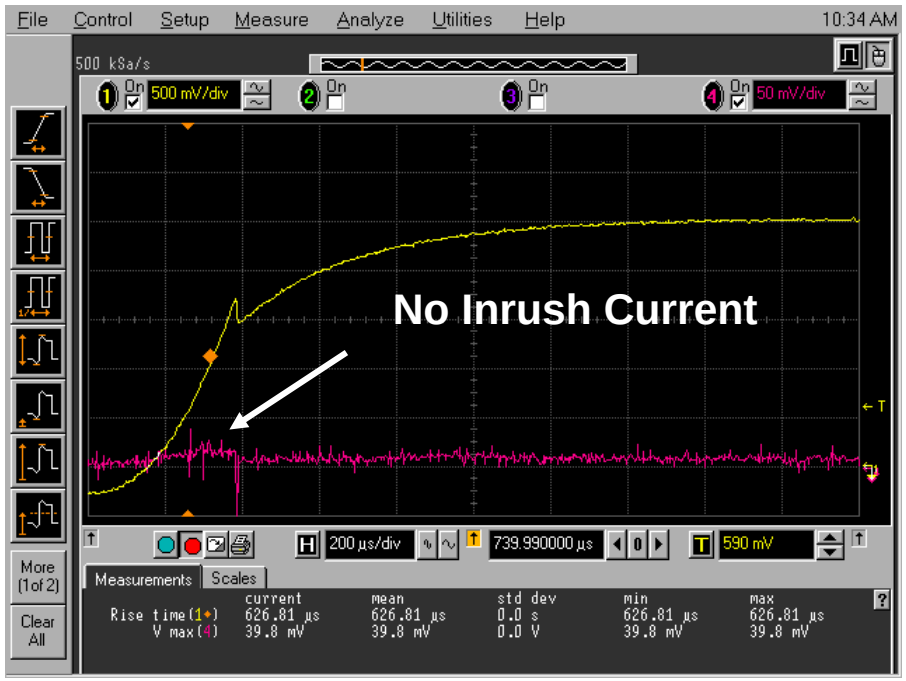
SRAM FPGA and SRAM-Hybrid FPGAs

- **May experience > 1 Amp spike**
- **Requires power sequencing**

System Power

Current





Actel Flash/Antifuse FPGAs

- **No power-up spike**

System Power

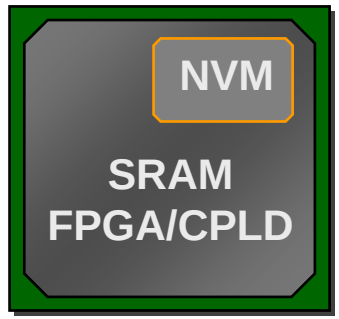
Current

Power-Up *Configuration Current*

- Volatile SRAM FPGAs have to be configured during system power-up
- During configuration, which lasts hundreds of microseconds, current may peak at over 100 mA and averages over 50 mA
- Flash and antifuse FPGAs are Level 0 live at power-up (LAPU) and do not require configuration

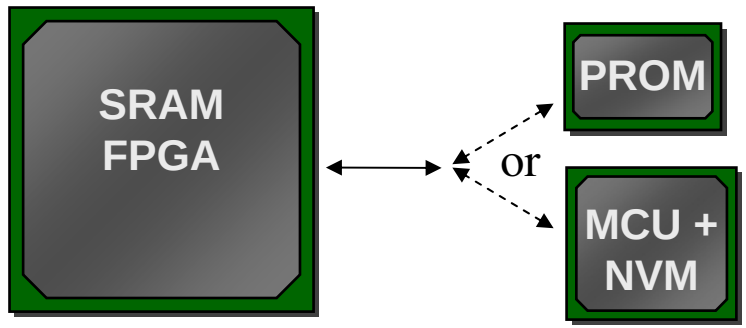
SRAM

Hybrid FPGAs/CPLDs – SRAM fabric loaded from NVM on-chip

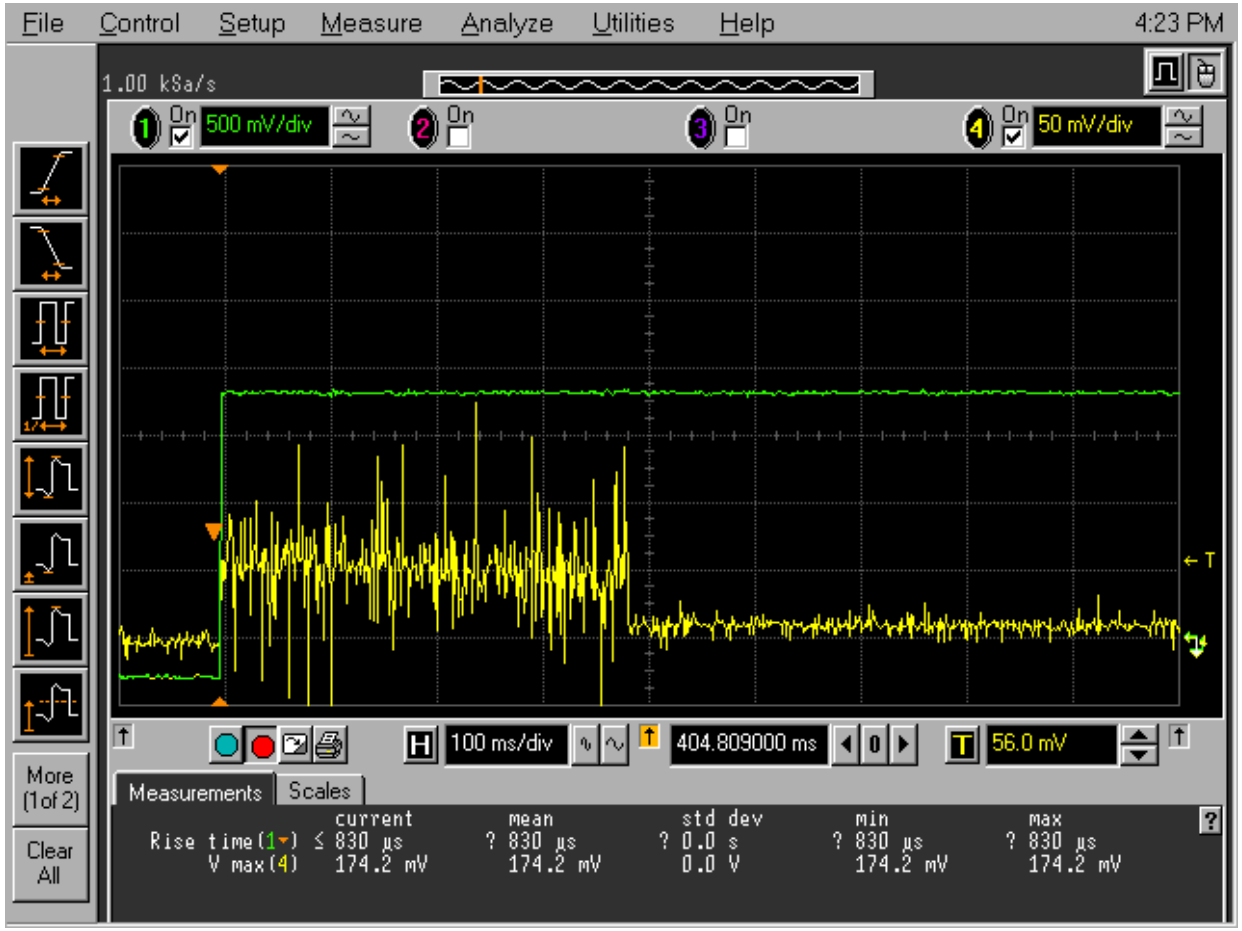


SRAM

SRAM FPGA with boot



Configuration Current
SRAM and SRAM Hybrid FPGAs

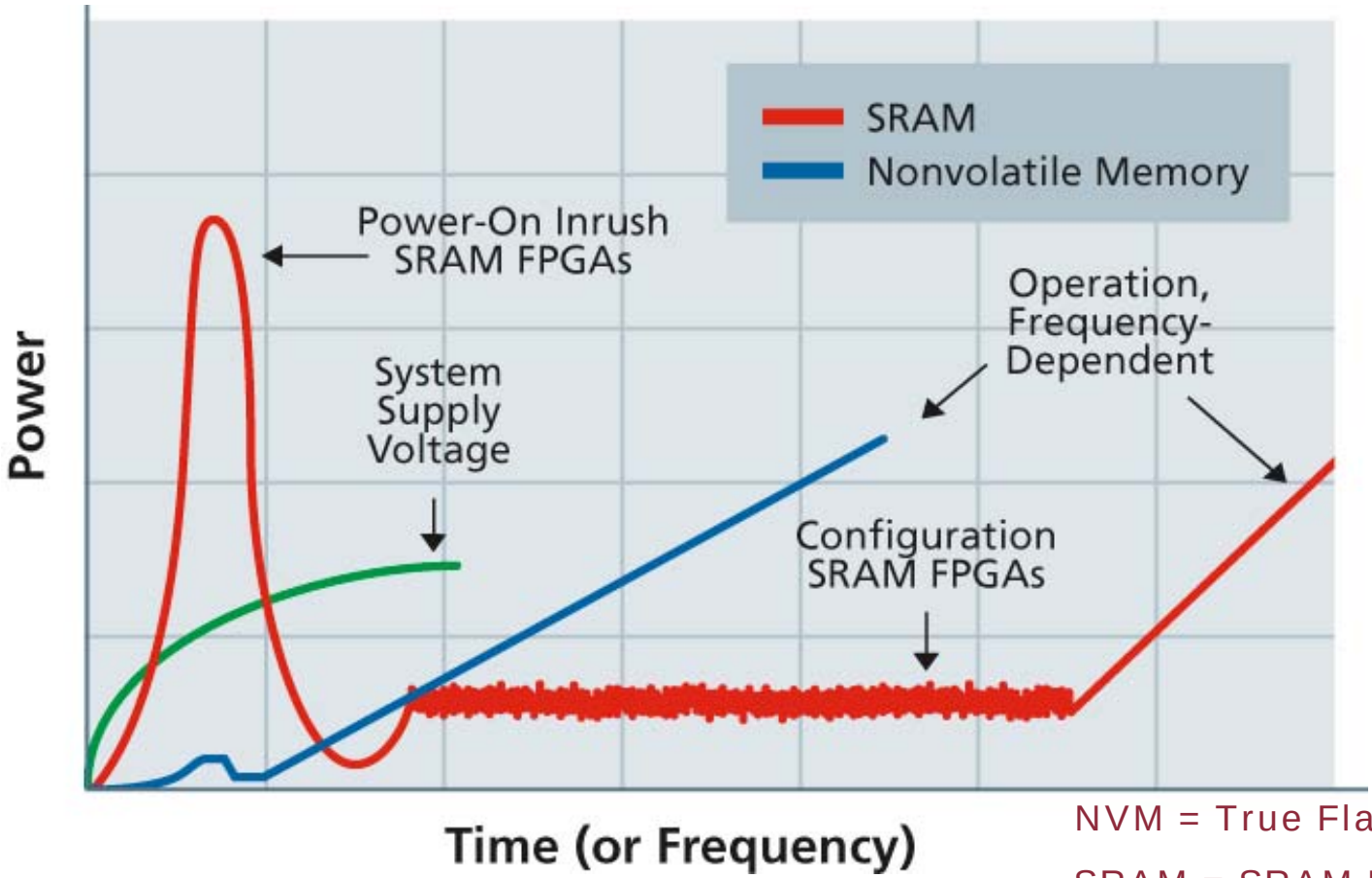


System Power

Current

- Configuration time hundreds of ms typically
- Configuration current hundreds of mA typically

System Power Power-Up



NVM = True Flash/Antifuse FPGAs

SRAM = SRAM FPGAs and SRAM Hybrid FPGAs

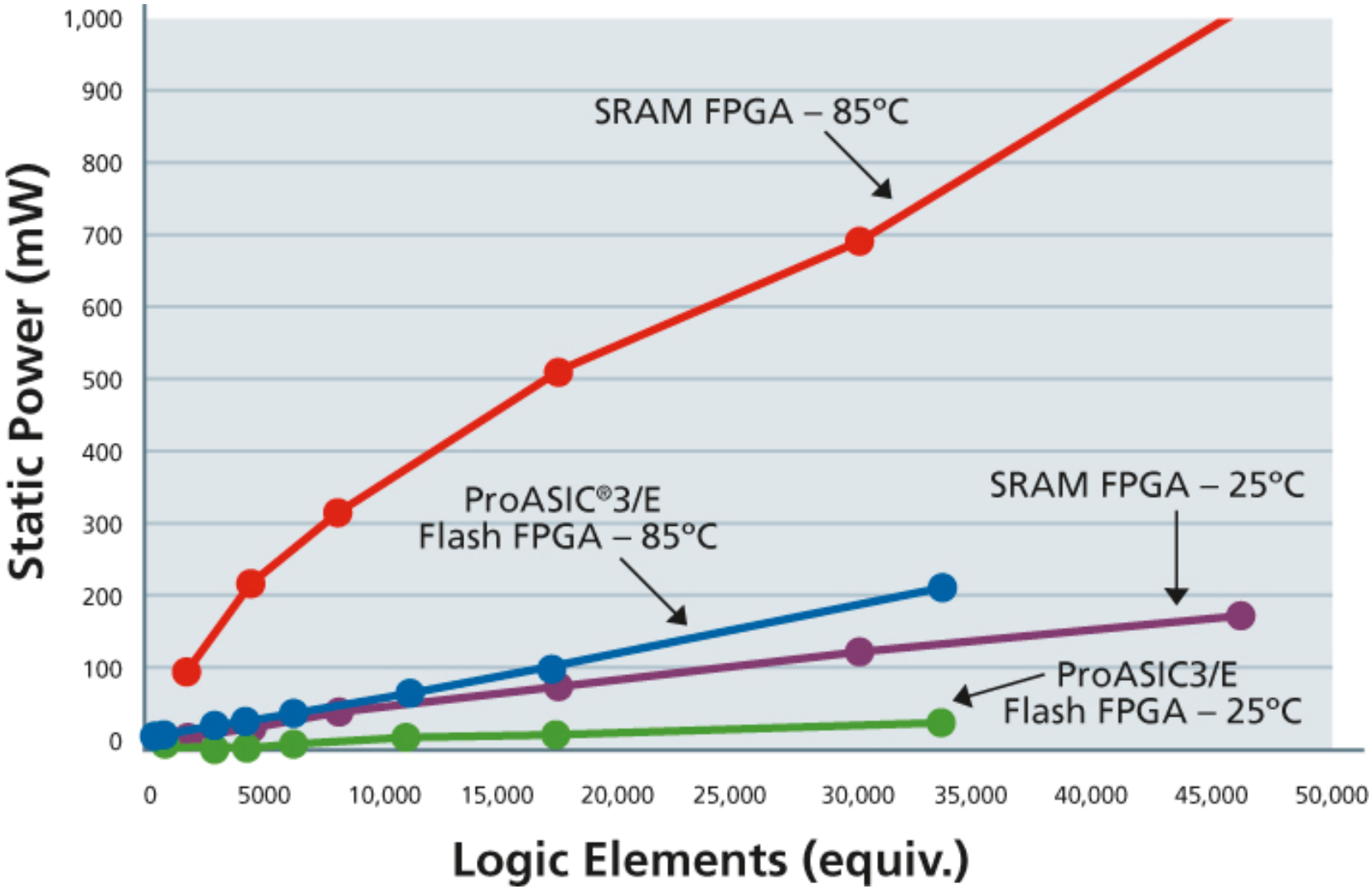
- Inrush power
- Configuration power

System Power Operation

Operation
Static Power

- Minimum power required to keep the device “powered-up” with the clock inputs not switching
- I/Os are drawing minimal power
- Some FPGAs offer a lower power mode feature that disables the I/O putting it into a sleep mode that further reduces static power
- Static power varies (sometimes dramatically) with temperature
- At 90-nm process technology, static power becomes the dominant power factor

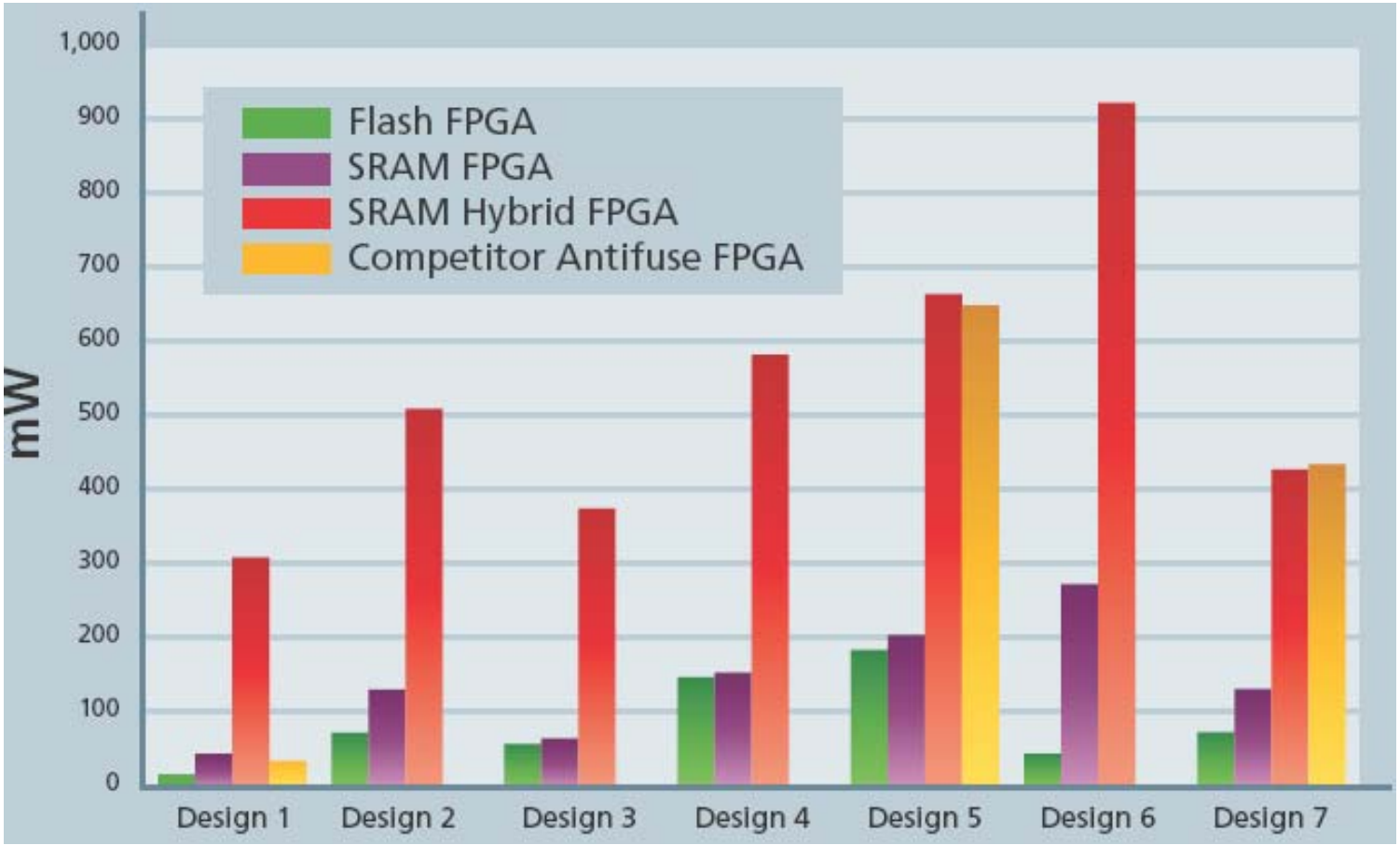
Static Current
SRAM and NVM FPGAs



Operation
Dynamic Power

- Power consumed when the logic cells are switching
- Power consumption increases with frequency and operating temperature
- Dynamic power varies by technology and architecture
- Major concern for heat dissipation and operating power consumption

Dynamic Power
SRAM and NVM FPGAs

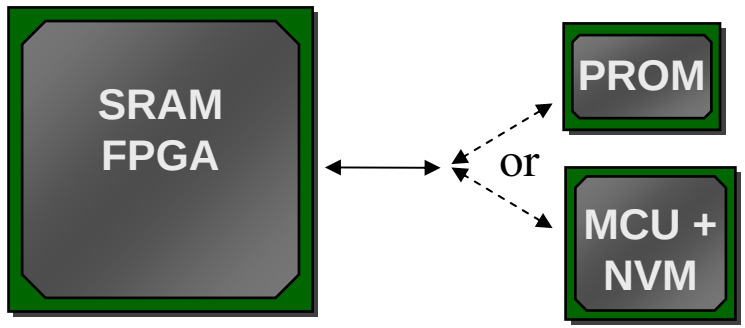


Operation
Sleep / Low Power Modes

- Few vendors offer ways to put the device in sleep mode
  - **Allow for lower power consumption than static**
- SRAM FPGAs
  - **Require reconfiguration**
    - **And power for reconfiguration**
  - **Long time to enter/exit low power mode**
  - **Require additional components**
- Flash FPGAs
  - **No need in reconfiguration**
  - **Enter/exit mode is quick**
  - **Ability to save state and restore**
  - **Flash*Freeze technology**

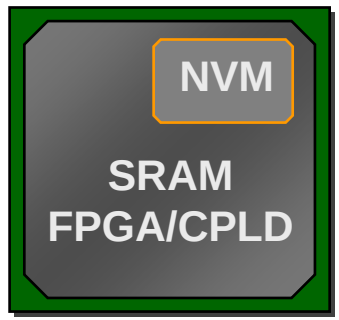
SRAM

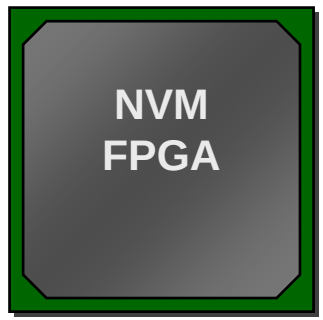
SRAM FPGA with boot



SRAM

Hybrid FPGAs/CPLDs – SRAM fabric Loaded from nonvolatile memory (NVM) on-chip





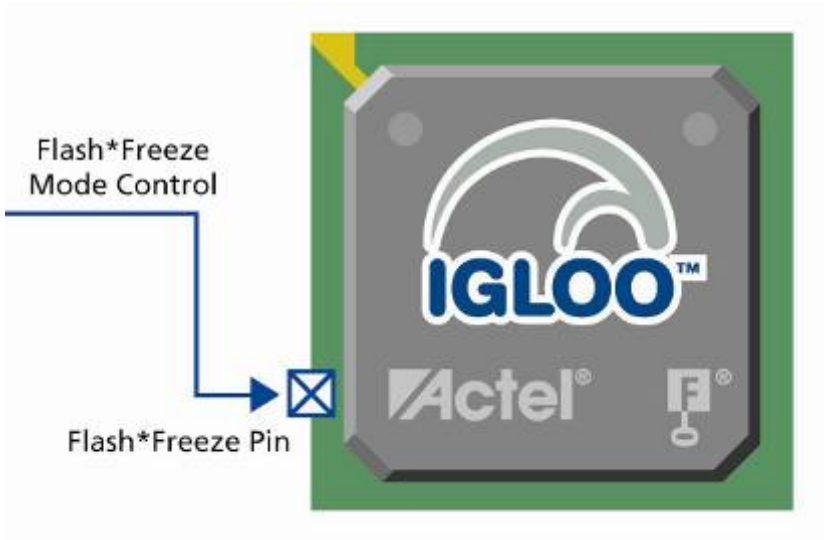
NVM

True Flash and antifuse FPGAs

Actel's Igloo FPGAs Flexible System Implementation

Flash*Freeze mode

- **Power consumption as low as 5 µW**
  - **Enter/exit within 1 µs via Flash*Freeze pin**
- **During Flash*Freeze Mode**
  - **No need to power off voltage**
  - **Freezes clocks and I/Os**
  - **Core registers and SRAM maintain state**
  - **'No' power consumed by I/Os, JTAG pins, PLL**



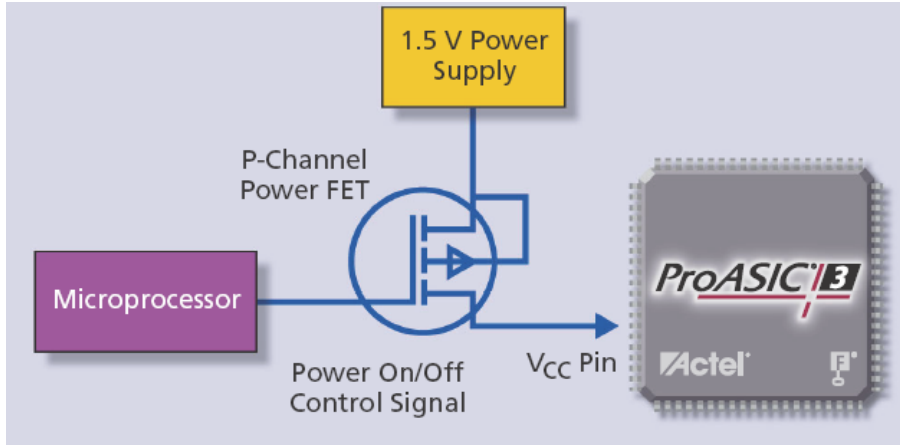
Low power active mode

- **Allows IGLOO devices to directly control system power**
- **Power consumption as low as 25 µW (Static)**
- **Slow (e.g., 32 kHz) or stop the clocks**
- **Part remains active in system**

IGLOO & ProASIC3 Flash FPGA Low Power modes

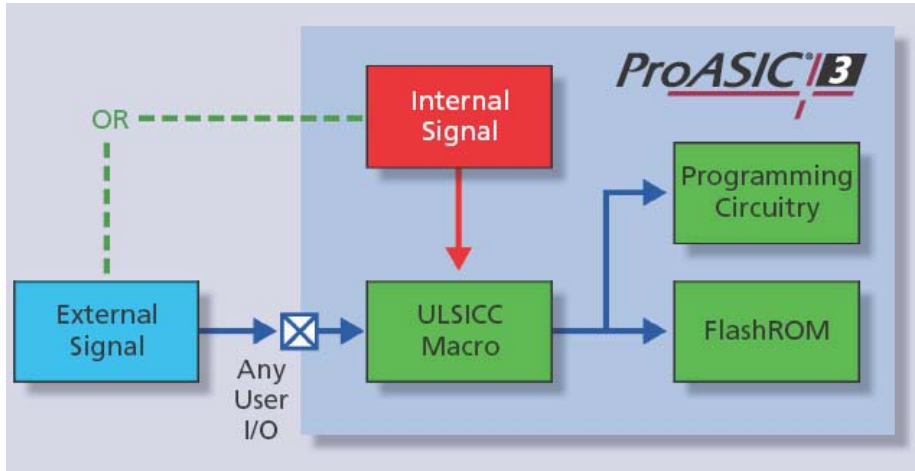
Sleep Mode

- **Power down the core, but leave the I/Os powered up**
  - **Optional: Save and load data from external memory**
- **Live at power-up capability of the device powers up ~50 µs typically**
- **Under 150 µW typical ProASIC3 devices**



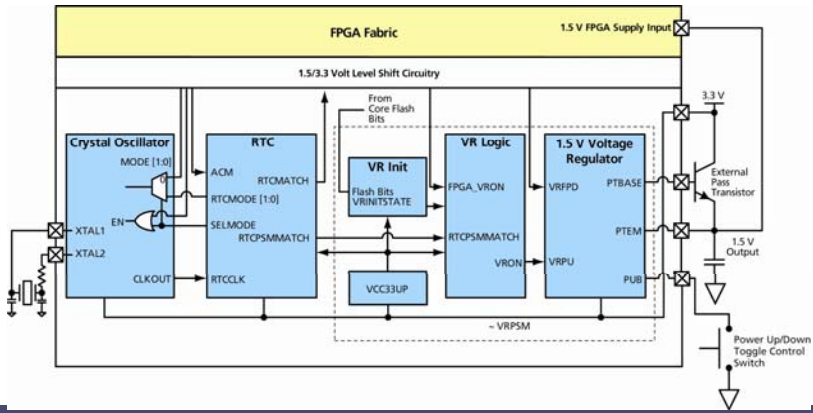
User Low Static Macro

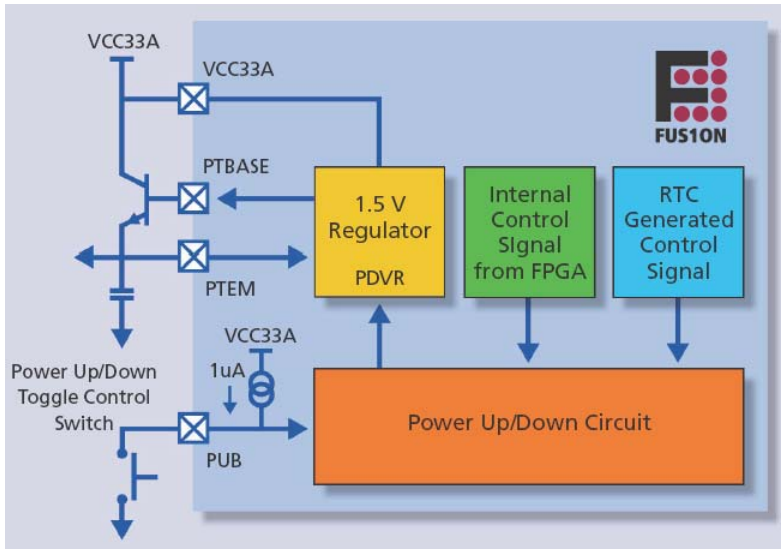
- **Device can be in active/ static modes**
- **Can be controlled internally or externally**
- **Static power consumption reduction of up to 30%**

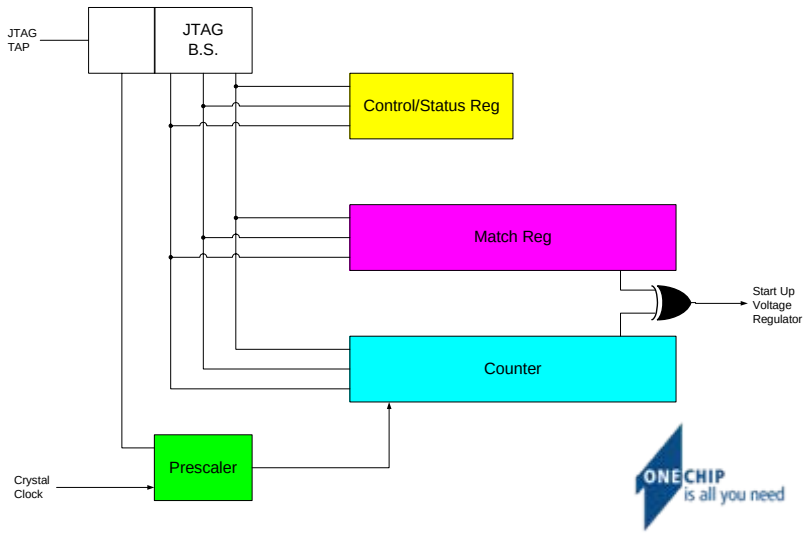


Fusion Flash FPGA Low Power modes

- Standby Mode
  - **FPGA array is fully powered down by the regulator**
  - **Oscillator and real-time counter (RTC) are active**
  - **Can wake from internal RTC or external trigger**
  - **Typical 350 µW**
- Sleep Mode
  - **FPGA array is fully powered down by the regulator**
  - **No other circuits are active**
  - **Needs external signal to wake up**
  - **Typical 15 µW**
- User Low Static Macro







Actel's IGLOO and ProASIC3 Power Modes Overview

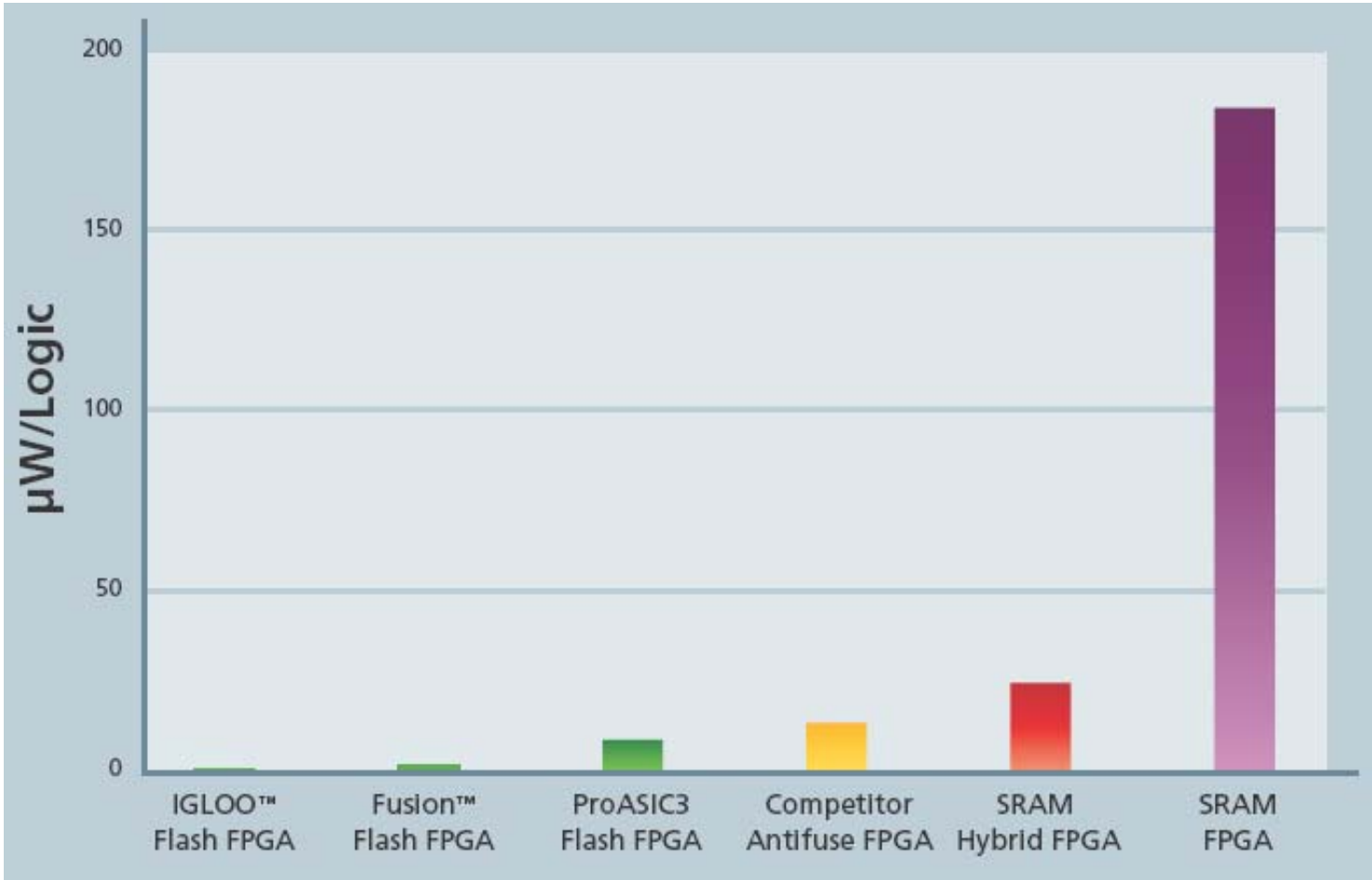
Mode		V_{CCI}	V_{CC}	Core	Clocks	To Resume Operation	Trigger
Active		On	On	On	On	None	-
Static	Flash* Freeze	On	On	On	On	Deassert Flash*Freeze pin	External
	Idle	On	On	On	Off	Initiate clock	External
Sleep		On	Off	Off	Off	V_{CC} cupply	External
Shutdown		Off	Off	Off	Off	V_{CC} and V_{CCI} supplies	External

- IGLOO Devices Only
- ProASIC3 and IGLOO Devices

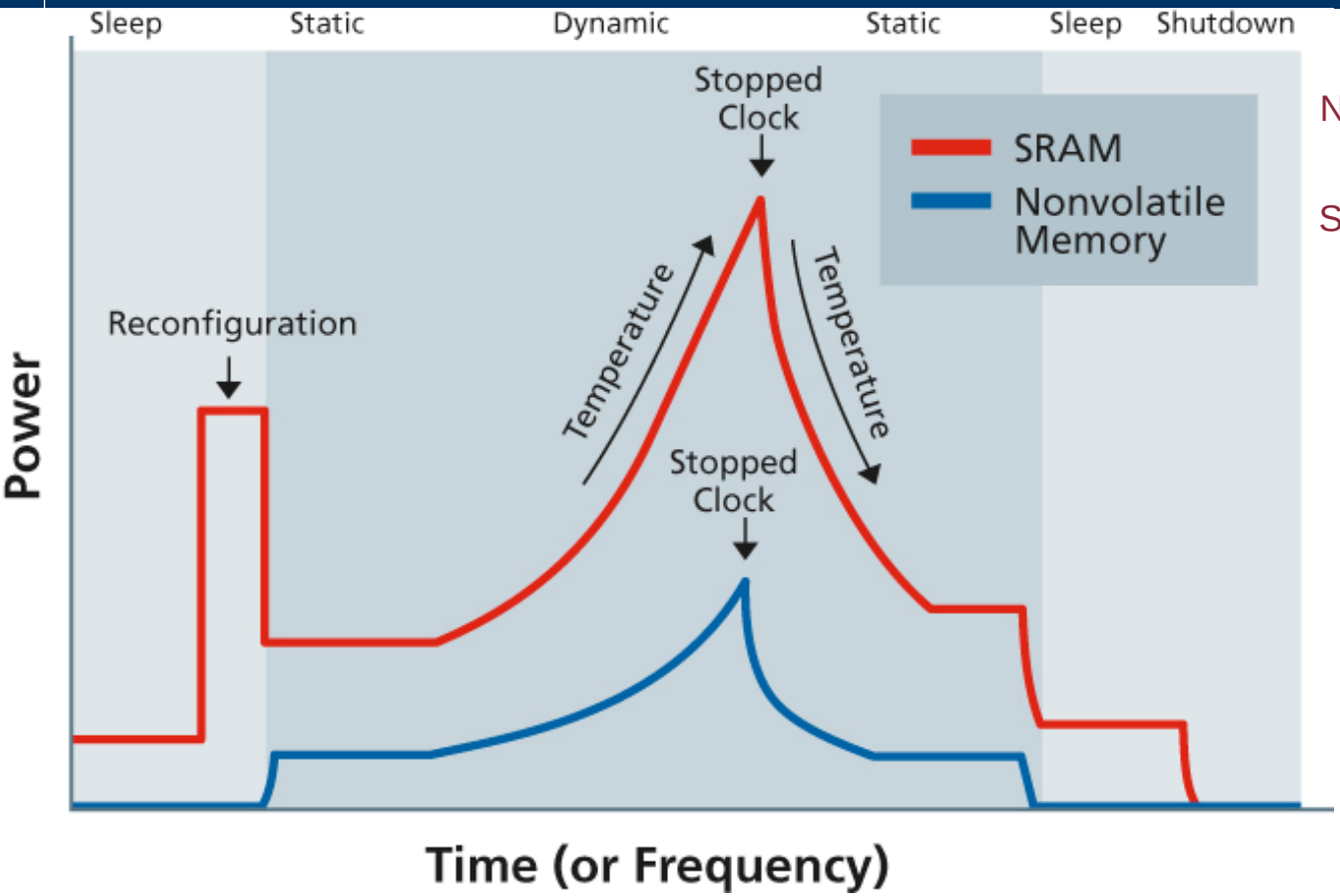
Actel's Fusion Power Modes Overview

Mode	3.3 V Supply	RTC	XTL OSC	1.5 V from V-Reg	Flash Memory	Core	Clocks	To Resume Operation	Trigger
Active	On	On	On	On	On	On	On	None	-
Static	On	On	On	On	On	On	Off	Initiate clock	RTC or External
Standby	On	On	On	Off	Off	Off	Off	Enable V-Reg to core	RTC or External
Sleep	On	Off	Off	Off	Off	Off	Off	Enable V-Reg to core	External (PUB)
Shutdown	Off	Off	Off	Off	Off	Off	Off	3.3 V Supply	External

Low Power Modes
SRAM and NVM FPGAs



System Power Operation



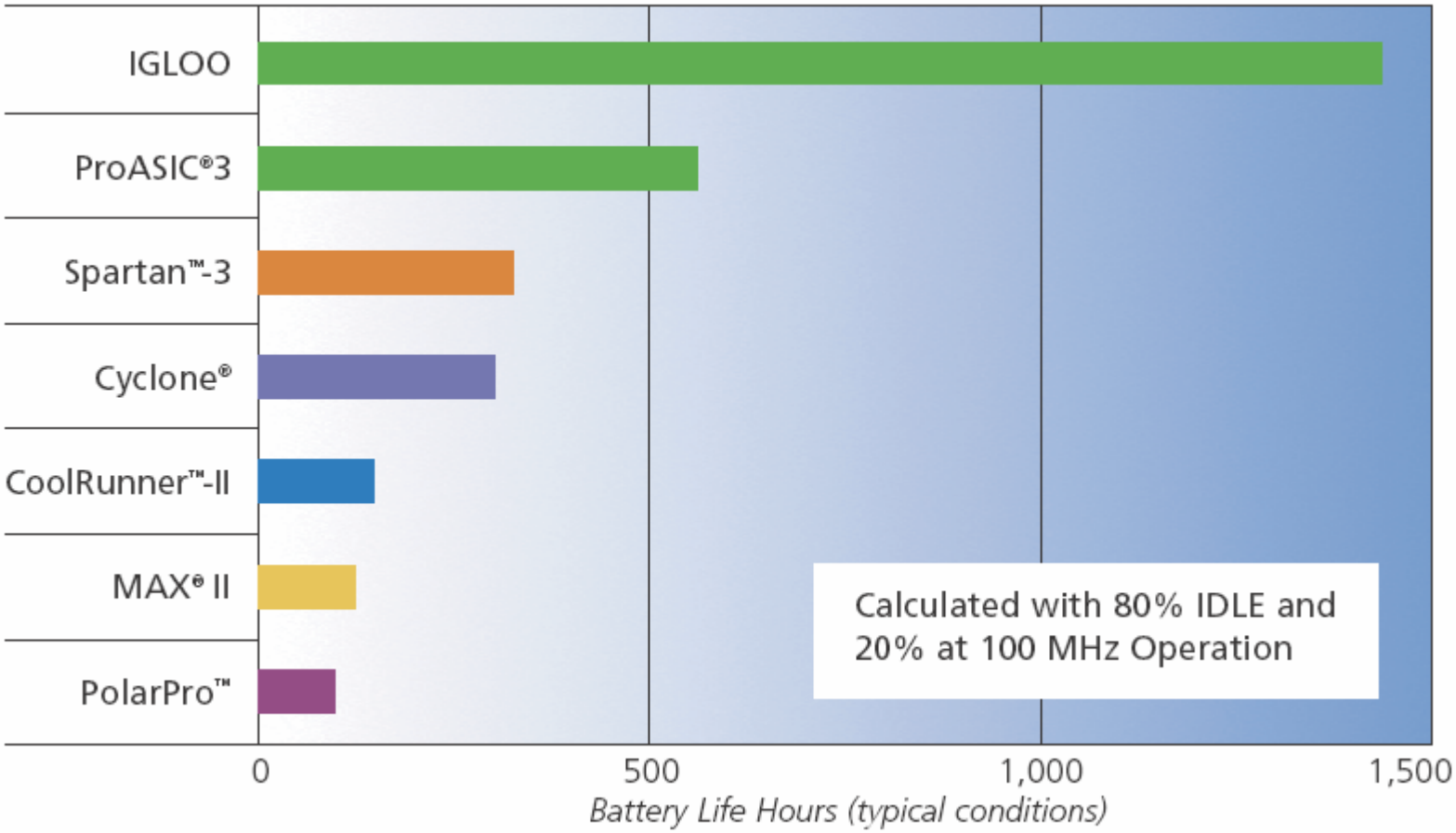
NVM = True Flash/Antifuse FPGAs

SRAM = SRAM FPGAs and SRAM Hybrid FPGAs

- Dynamic Power (high and room temperatures)
- Static Power (high and room temperatures)
- Sleep Power

System Power Summary

Battery Life Experiment



Power Support Tools

- Most FPGA suppliers have available tools to estimate power consumption
- Power Calculators
  - **Estimates average power consumption**
  - **Reports static and dynamic power**
  - **Is fully integrated in EDA design tool**
  - **Extracts data from the physical layout of the design**
- Power Spreadsheet
  - **Spreadsheets are intended to be a rough power estimation**
  - **They have a reduced number of parameters**
- Power Calculator Comparisons
  - **Input parameter assumption vary between manufacturers**
  - **Application support is available to help customers make an accurate comparison.**

Summary

- FPGAs have a unique power profile that varies with different FPGA technology.
- Actel's Flash and antifuse FPGAs offer the best power characteristics:
  - **No inrush current, No configuration current**
  - **Power optimized technology and architecture**
  - **Effective low power modes**
  - **Better power consumption over temperature**
- Flash FPGAs are best for battery-operated applications
  - **Single-chip**
  - **Reprogrammability**
  - **Low unit cost and total system cost**
  - **Small footprint packages**
  - **Flash*Freeze technology with IGLOO low power FPGAs**
- ... and Lowest Total System power
- Actel Power Resource Center
  - **http://www.actel.com/products/rescenter/power/**