Actel's SX Family of FPGAs:
A New Architecture for High-Performance Designs

A Technology Backgrounder

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
April 20, 1998

Actel Corporation is dedicated to providing the best possible programmable logic solutions, giving logic designers the capability to successfully move up to higher capacity designs with confidence.

Introduction

For several years now, industry analysts have noted a strong trend in which field programmable gate arrays (FPGAs) have transitioned from being strictly a prototyping tool, to a necessary component for a wide range of production-volume, end-use applications. There are several reasons for this trend, including lower FPGA costs, increasing FPGA performance, and perhaps most important, a driving necessity for the fast time-to-market enabled by FPGA technologies.

Yet even as FPGAs reach into these markets, design requirements are becoming more stringent. Today, applications in telecommunications, networking, computing and other markets require low-cost, high-performance devices that integrate more functionality and use less power than ever before. Time-to-market windows are also shrinking, prompting many designers to seek the simplest possible architecture upon which to base their designs.

In the past, high performance requirements would have been met by one of two strategies. In the first, the designer would partition the design into several components — typically including large FPGAs and high-performance complex programmable logic devices (CPLDs). However, this strategy is costly in terms of design time, board space, and component expense, and it defeats the requirement for higher integration. The alternative strategy would have been to implement the design in an ASIC, thereby achieving the design's performance goals but at the expense of significant product time-to-market delays and NRE charges.

Today, Actel's new SX Family of FPGAs deliver the best of both strategies, providing all of the cost, performance, power, and time-to-market requirements in a single high-performance, cost-effective programmable logic device. The SX features a revolutionary new architecture, enabling dramatic reductions in die size and cost, design time, and power utilization, while increasing device performance and integration to levels not currently achieved by any other FPGA architecture.

SX Family Architecture

The SX Family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of markets, including computing, networking, telecommunications, instrumentation, medical, and industrial control and automation. The SX Family architecture is fundamentally different from any other FPGA architecture in three areas:

1. Programmable Interconnect Element
2. Logic Module Design
3. Chip Architecture

Programmable Interconnect Element. Actel's new SX Family provides much more efficient use of silicon by moving routing and interconnect resources from the area between logic modules to the Metal 2 (M2) and Metal 3 (M3) layers (see Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules. At the same time, it allows Actel to achieve a smaller die size — and lower die cost — by packing logic modules into the smallest possible area.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX Family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible as it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

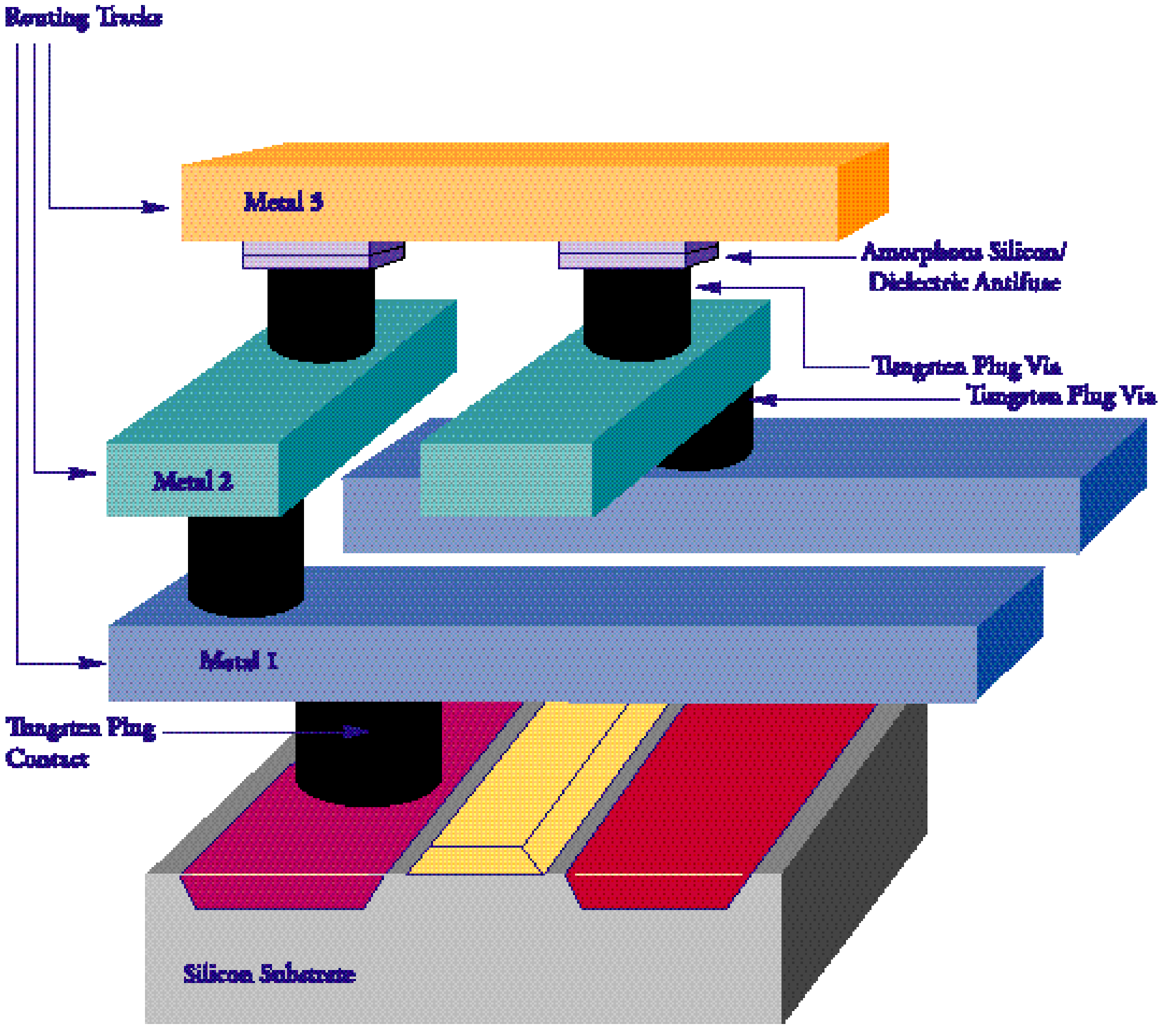

Figure 1. SX Family Interconnect Elements.

By placing the routing and interconnect resources above the logic grid, Actel has already accomplished what no SRAM-based FPGA architecture can do: it has dramatically decreased the die size of the FPGA at any given density, which markedly reduces the cost of the FPGA. Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

Logic Module Design. The SX Family architecture has been called a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing (see Figure 2). Actel provides two types of logic modules, the *R-cell* and the *C-cell*.

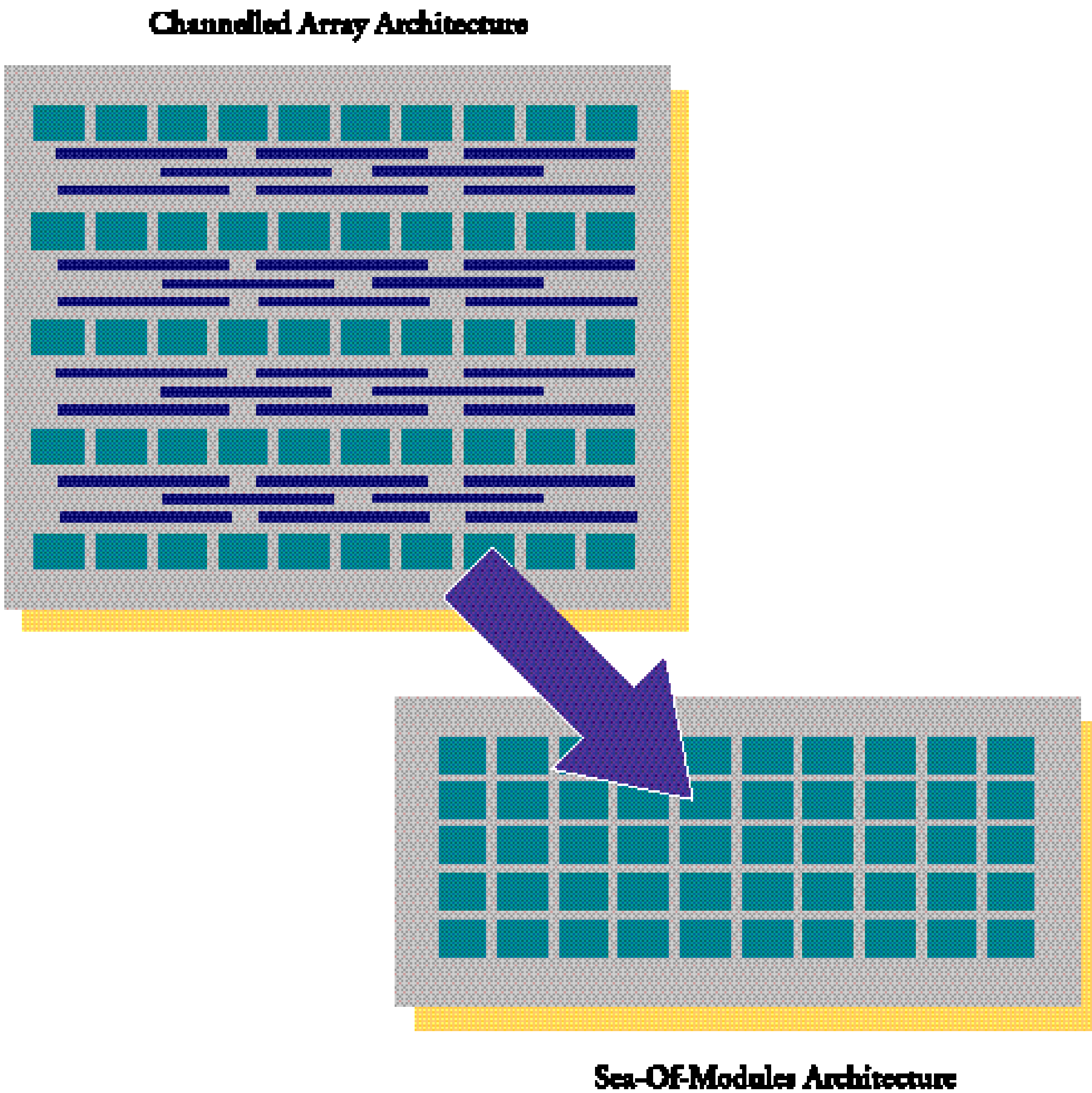

Figure 2. Channelled Array and Sea-of-Modules Architectures.

The R-cell (or register logic module) contains a flip-flop featuring more control signals than in previous Actel architectures, including a clear, preset and clock enable. The R-cell (Figure 3A) registers feature programmable clock polarity, selectable on a register-by-register basis. This provides the designer with additional flexibility while making the overall design more synthesis-friendly.

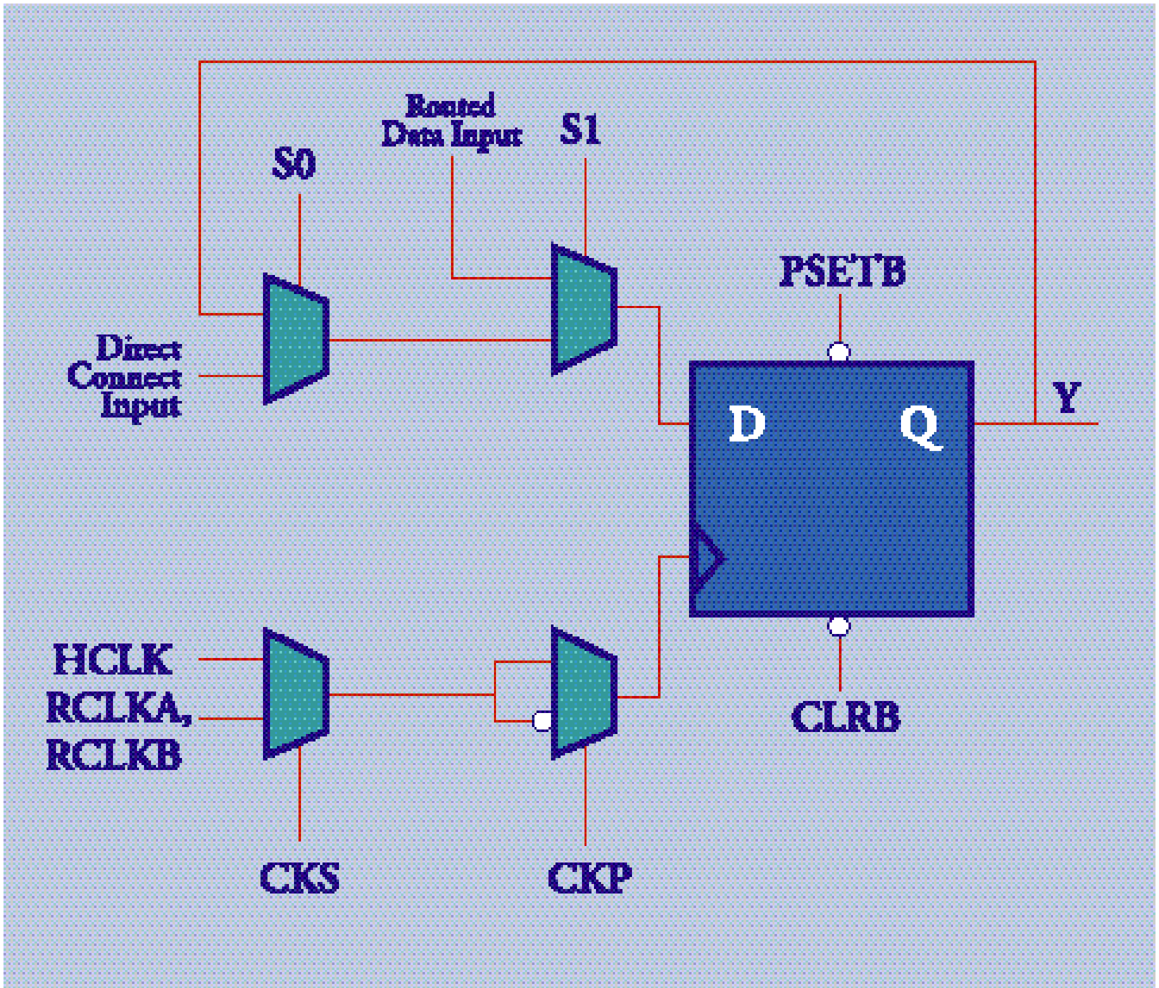

Figure 3A. R-Cell.

The C-cell (or combinatorial logic module) implements all 3-input and some 4-input and 5-input functions. Each C-cell (Figure 3B) features an inverter function, which represents a significant breakthrough: in the past, each inverter function would require the addition of another entire logic module.

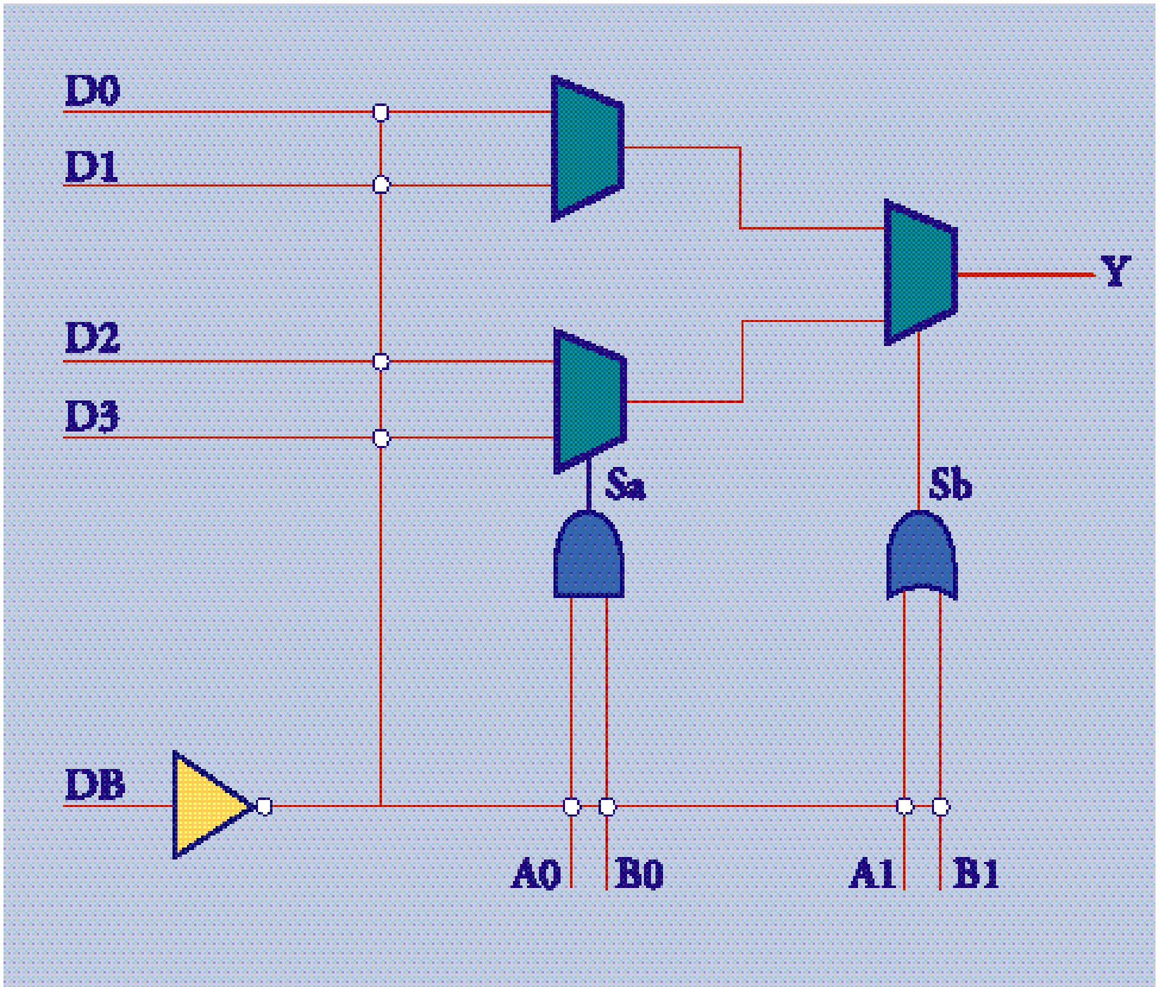

Figure 3B. C-Cell.

By integrating an inverter into each logic module, Actel has dramatically increased the number of combinatorial functions which can be implemented in a single module from 800 options to more than 4,000. At the same time, the reduction in logic resource requirements enabled by the C-cell's inverter makes the device extremely synthesis-friendly, simplifying the overall design and reducing synthesis time. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays.

Chip Architecture. The SX Family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization. Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (see Figure 4). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature significantly more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

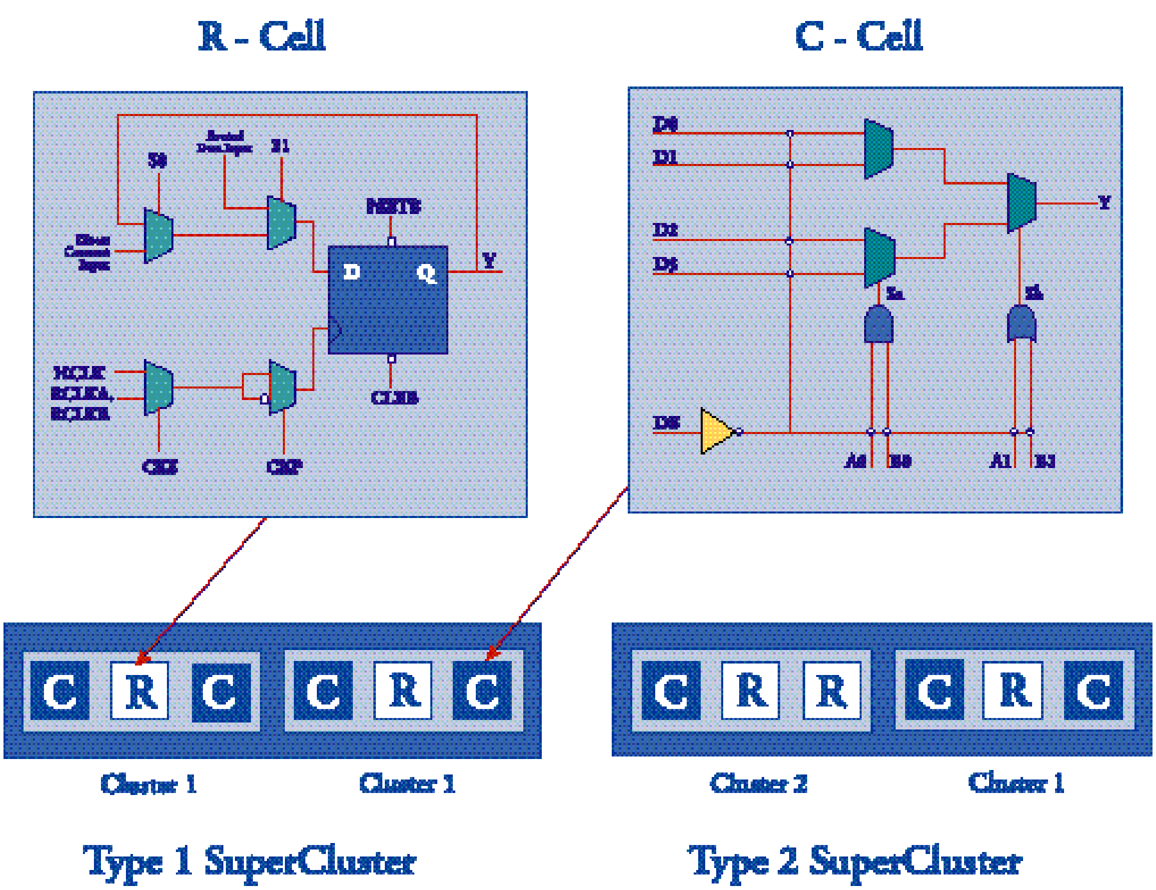

Figure 4. Cluster Organization.

Routing Resources. Clusters and SuperClusters can be connected through the use of two innovative new local routing resources called *FastConnect* and *DirectConnect* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (see Figure 5A and Figure 5B). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

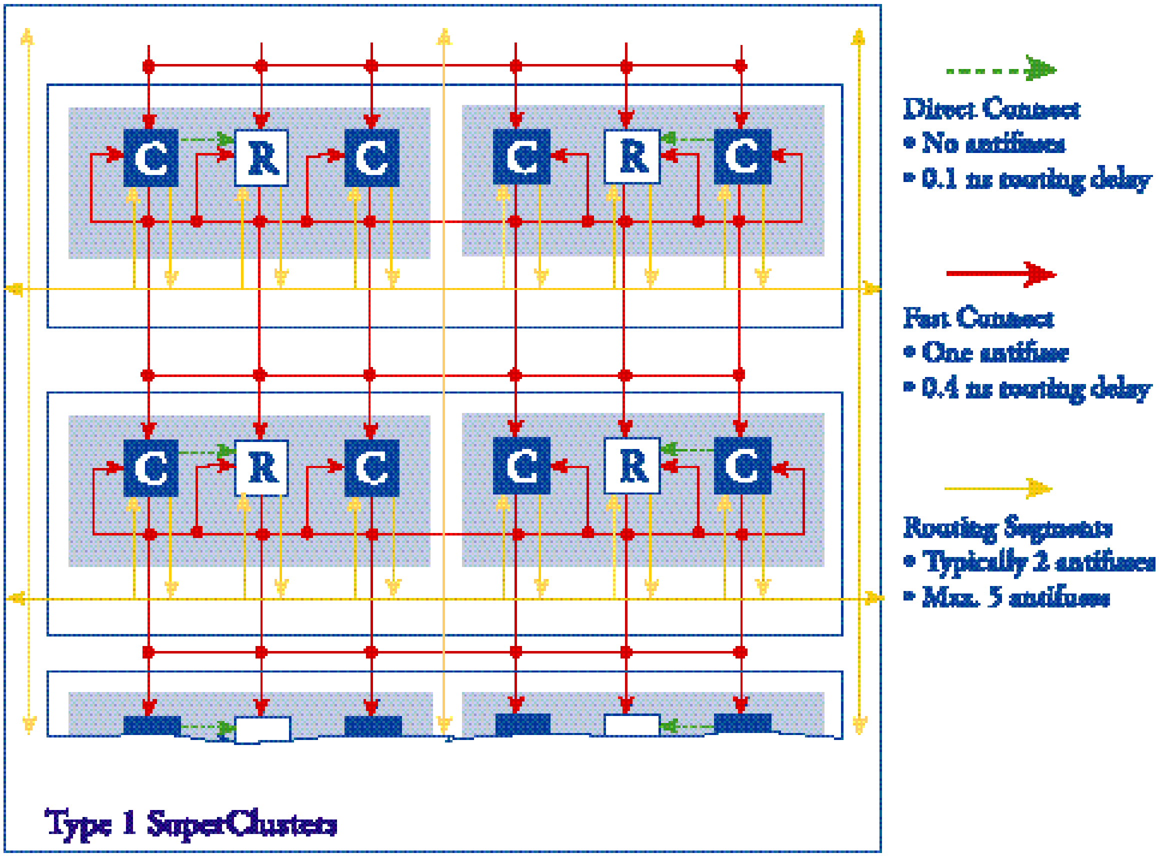

Figure 5A. DirectConnect and FastConnect for Type 1 SuperClusters.

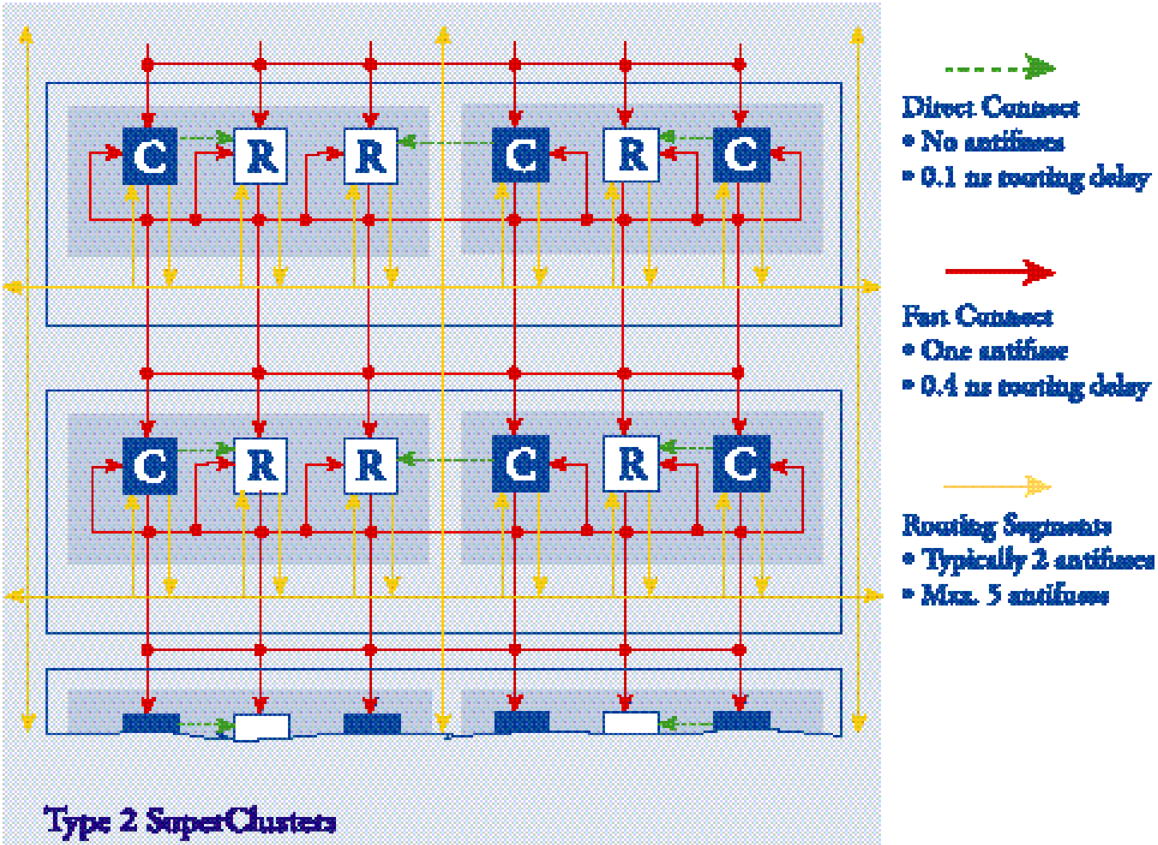

Figure 5B. DirectConnect and FastConnect for Type 2 SuperClusters.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation between 0.3 and 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as *segmented routing* and *high-drive routing*. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path was chosen based on 10-plus years of experience designing and developing antifuse FPGAs for a variety of applications.

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hard-wired into the device. The remaining two clocks (CLKA, CLKB) are global clocks that must be routed into the design using place and route tools. In combination, these clocks enable increased design flexibility, supporting the integration of multiple CPLDs into a single SX FPGA.

Other Architecture Features

Technology. Actel's SX Family of FPGAs is implemented in high-voltage twin-well CMOS using three layers of metal and 0.35 micron design rules (moving quickly to 0.25 micron). The M2/M3 antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals.

Performance. The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the Actel SX Family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs which previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time-to-market. Using timing-driven place and route tools, designers can achieve highly deterministic device performance.

With SX devices, designers can achieve a higher level of performance without recourse to complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code.

I/O Modules. Each I/O on an SX device can be configured as an input, an output, a tri-state output, or a bi-directional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 4.0 ns, and external set-up time as low as 1.4 ns (Figure 6). By including simple I/Os, the SX Family saves die size and cost. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reducing overall design time.

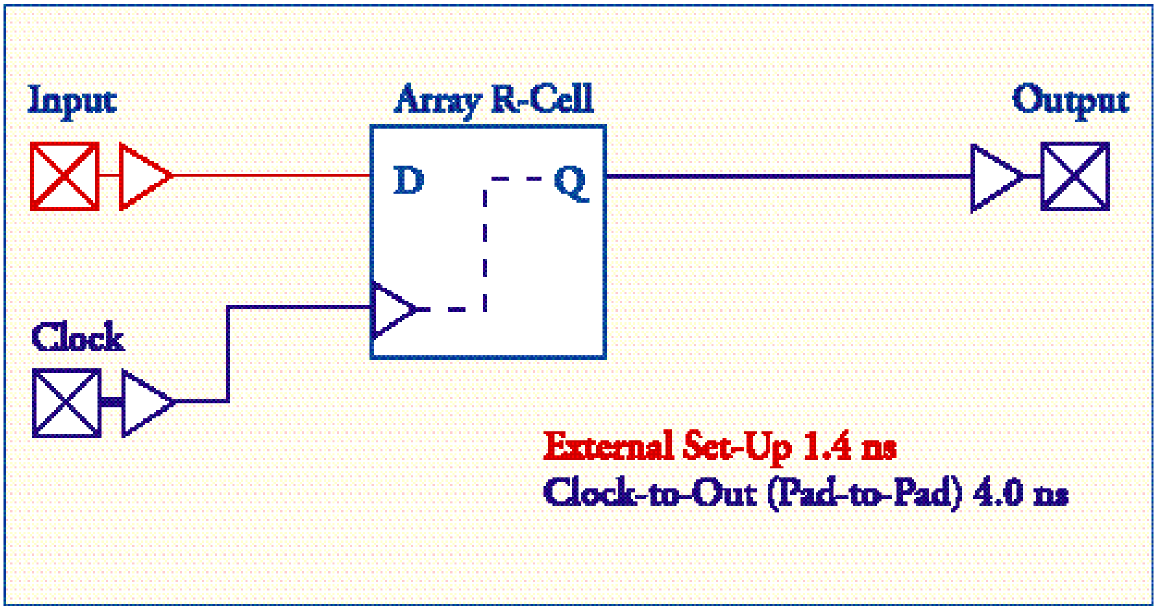

Figure 6. Fast On-Chip/Off-Chip Performance.

Power Requirements. The SX Family supports 3.3-volt operation and is designed to tolerate 5-volt inputs. Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path, and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as an SRAM or EPROM does), thereby making it the lowest-power architecture on the market.

JTAG. All SX devices feature hard-wired IEEE 1149.1 JTAG Boundary Scan Test circuitry.

Design Tool Support. As with all Actel FPGAs, the new SX Family is fully supported by Actel's Designer Series development tools, which include:

- DirectTime for automated, timing-driven place and route;
- ACTgen for fast development using a wide range of macro functions; and
- ACTmap for logic synthesis.

Designer Series supports industry-leading VHDL- and Verilog-based design tools, including synthesis tools from industry leaders such as Exemplar Logic, Synplicity, and Synopsys.

In addition, the SX Family is supported by Actel's new Silicon Explorer diagnostic and debugging tool kit. Silicon Explorer dramatically reduces verification time from several hours per cycle to a few seconds by enabling real-time, in-circuit debugging. Silicon Explorer includes:

- Probe Pilot, a high-speed signal acquisition and control tool that samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Probe Pilot features 18 probing channels and connects to the user's PC via a standard serial port connection.

- Diagnostic software, which includes turns the PC into a fully-featured, 100 MHz logic analyzer for easy graphical analysis of waveforms.

Silicon Explorer probes 100 percent of the device circuitry using Probe Pilot's powerful, 18-channel signal acquisition capability. Individual bugs are then isolated and passed to the user interface, providing the user with complete waveform data.

SX Family Overview

Actel's SX Family of FPGAs is currently planned to include four devices in a variety of package options, including PLCC, PQFP, VQFP, TQFP, CQFP and BGA. Table 1 provides an overview of the SX Family, illuminating its capacity to integrate multiple CPLDs while maintaining a lower cost-per-gate and offering higher performance.

Part Number	A54SX08	A54SX16	A54SX32	A54SX64
Capacity (Gates)	8,000	16,000	32,000	64,000
JTAG	Yes	Yes	Yes	Yes
Maximum I/O	129	176	246	340
Dedicated Flip-Flops	256	528	1,080	2,160
Combinational Logic Cells	512	924	1,800	3,600

Table 1. SX Family Overview.

Design Examples

In actual customer designs, Actel's SX Family has proved to be the only programmable logic capable of operating at design speeds in 66 MHz PCI and gigabit Ethernet designs. In both cases, the device allowed designers to bring their systems to market much faster than they would have otherwise achieved.

Actel's SX Family of FPGAs is also an excellent platform for implementing glue logic on high-speed microcontrollers such as the Intel i960 and other high-performance RISC and CISC microprocessors. The device's extremely fast propagation delay makes it a highly-suitable candidate for parity generators used in very fast networks. The SX Family's SuperCluster module organization easily handles wide fast designs such as address decoders. As shown in Figure 6, a 24-bit address decoder utilizes less than two full SuperClusters and requires less than 2 ns per instruction.

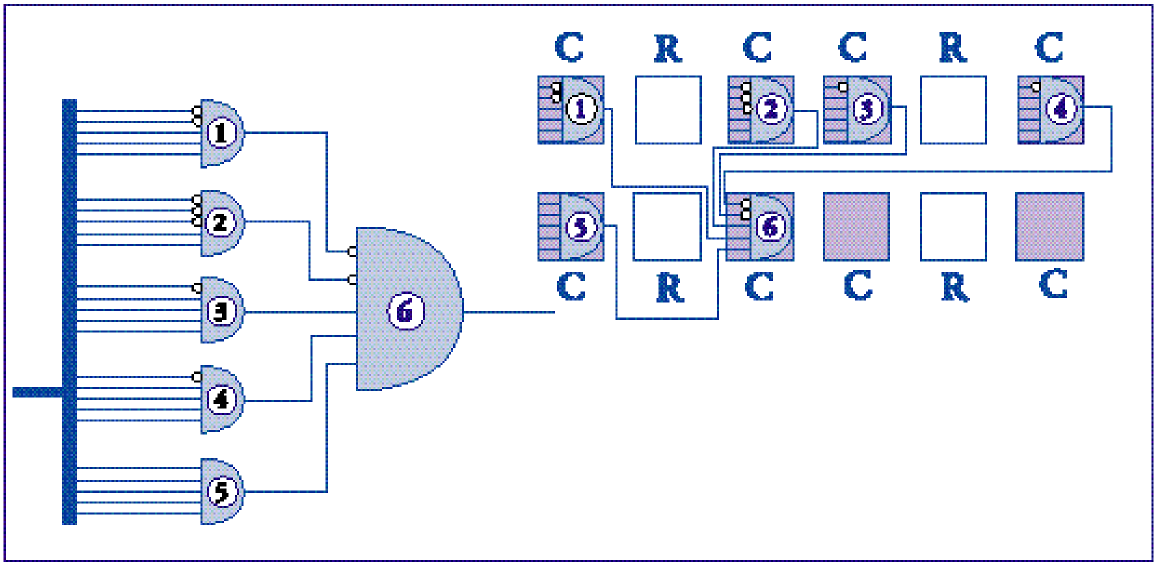

Figure 7. 24-Bit Address Decoder Example.

A 9-bit parity generator can be implemented in just one SuperCluster, with a 2 ns propagation delay, as shown in Figure 8.

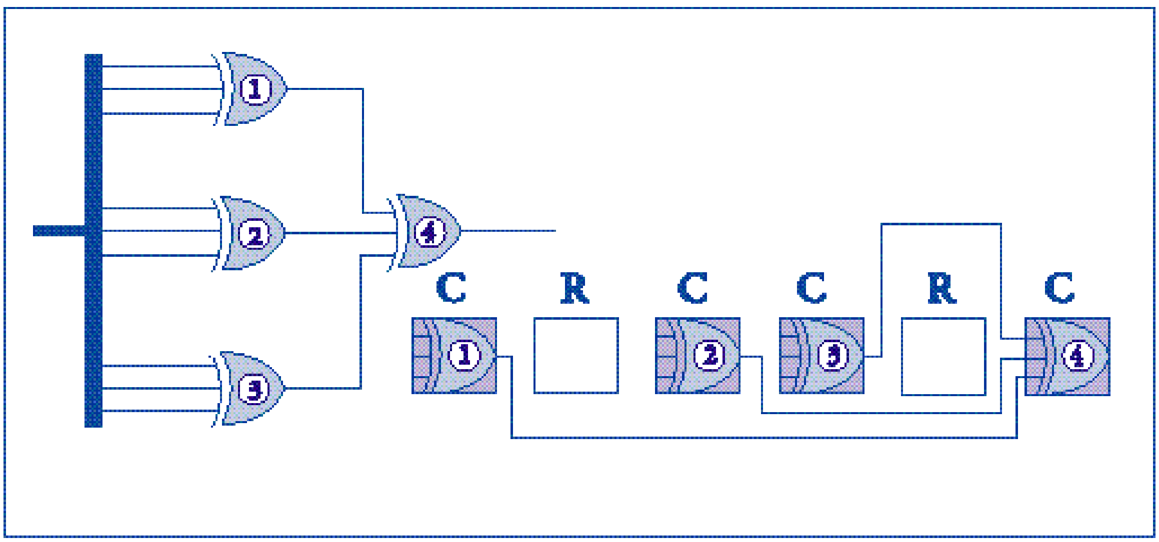

Figure 8. 9-Bit Parity Generator Example.

Conclusion

Actel's new SX Family is a revolutionary new FPGA architecture that provides extremely fast performance in the smallest possible die size for a given design (compared to other FPGA architectures). Less expensive than an ASIC at moderate volumes, Actel's SX family integrates the performance and functionality of multiple CPLDs into a single field programmable device. The expanded functionality enabled by the SX family's unique module design, coupled with the efficiency and performance provided by its carefully constructed module organization and routing resources, are the best and latest result of many years of experience designing fast, efficient, low-cost FPGAs. SX FPGAs provide a level of integration and power savings that will enable the designer to realize significant reductions in design costs and time-to-market. Actel's new SX Family of FPGAs provide an optimal platform for many new applications in telecommunications, networking, computing and other markets.

—End—