

# Power Cycling of RTSX-S Devices

## Introduction

Power cycling may be defined in various terms, based on different applications. In this application note, power cycling refers to consecutive power-up/down sequences of array and I/O voltage supplies of RTSX-S devices ( $V_{CCA}$  and  $V_{CCI}$ ). In general, RTSX-S devices do not require any specific sequence at power-up. However, an improper power cycling sequence may result in a significant "inrush" standby current ( $I_{CCI}$ ) on the I/O power plane ( $V_{CCI}$ ). It is important to differentiate between power cycling and the initial power-up of the device, since the inrush current phenomenon appears only at power cycling and not at initial power-up.

Even though the inrush current,  $I_{CCI}$ , does not affect the reliability of RTSX-S devices, designers may wish to minimize or eliminate it to reduce the cost of the system power management circuit. Actel has conducted an extensive series of measurements to characterize the inrush current phenomenon during power cycling with specific sequencing. This application note briefly discusses the fundamentals of the inrush current phenomenon and offers recommendations to eliminate the inrush current during power cycling. For more technical details on the inrush current phenomenon, refer to the [Actel RT54SX-S Particular Power Cycling Inrush Current Phenomena](#) paper, presented at the 2003 MAPLD conference.

The RTSX-S device family (including RT54SX32S and RT54SX72S devices) was produced by the MEC wafer foundry (now discontinued). The RTSX-SU device family (including RTSX32SU and RTSX72SU devices) is produced by the UMC wafer foundry.

While  $I_{CCI}$  inrush current phenomenon can result due to improper power cycling sequence for the RTSX-S devices, the equivalent RTSX-SU device family has eliminated the inrush current phenomenon. The RTSX-SU (UMC) devices are available now. Contact local sales office or distributors for ordering information.

## Power Cycling and Inrush Current Phenomenon

If the following power cycling sequence is applied, a significant amount of inrush current on the order of a few amps is observed on the  $V_{CCI}$  power supply.

1. Power up  $V_{CCI}$  and  $V_{CCA}$  of an RTSX-S device in any sequence.
2. Power down the device ( $V_{CCI}$  and  $V_{CCA}$ ).
3. Power up the device again immediately (within seconds) with  $V_{CCI}$  first and  $V_{CCA}$  second.

The inrush current does not occur if the characteristic (such as  $V_{CCI}$  and  $V_{CCA}$  sequence) of the power cycling is different from the above steps. [Figure 1](#) shows an example of the power cycling sequence which will result in high inrush current ( $I_{CCI}$ ).

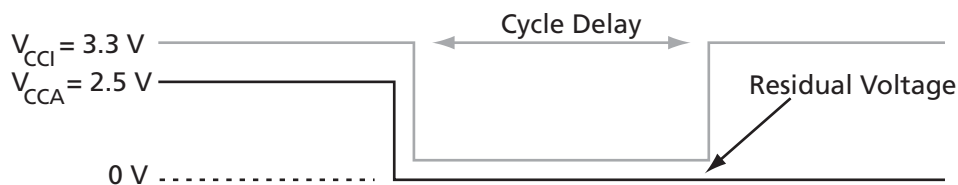


Figure 1 • Improper Power Cycling of RTSX-S Devices

In order to understand the nature of the  $I_{CCI}$  inrush current, the I/O configuration of RTSX-S devices at power-up/down must be understood. Figure 2 illustrates a simplified diagram of the RTSX-S I/O structure, where the PMPOUT signal is the device charge pump output, and T1 and T2 are the driving CMOS transistors of the output buffer.

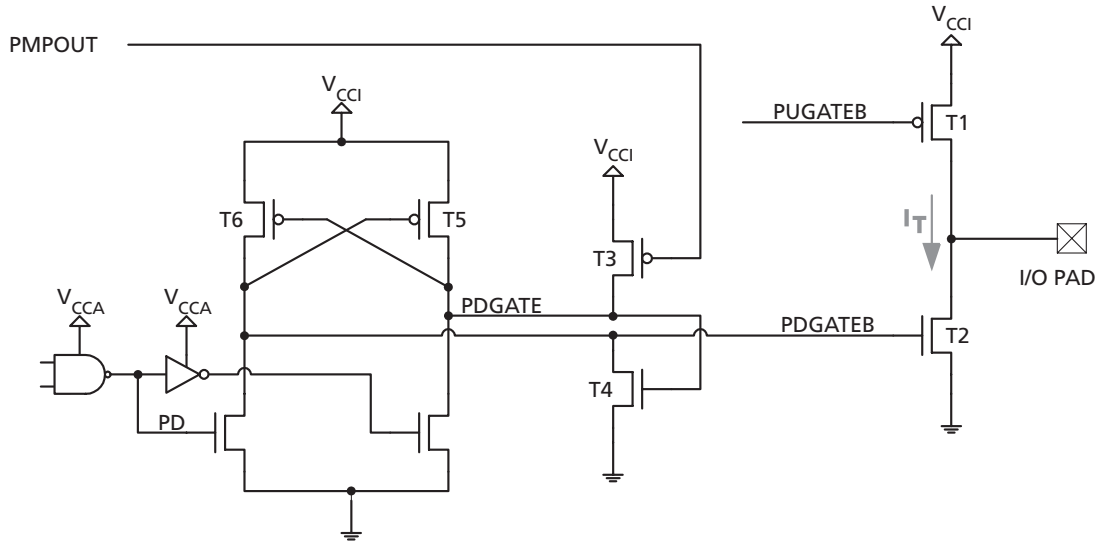


Figure 2 • Simplified I/O Diagram of RTSX-S Devices

At the initial power-up of RTSX-S devices, the PMPOUT signal is in the Low state. Hence, T3 and consequently T4 are On. As a result, PDGATEB is in the Low state at initial power-up, which in turn keeps T2 in the Off state. A circuit similar to the driving PDGATEB (Figure 2) drives PUGATEB. Therefore, at initial power-up of the device, both T1 and T2 are Off and the I/Os are in tristate mode. Once power-up is completed, PMPOUT is set to state High by the charge pump circuit of the device. The state of PDGATEB and PUGATEB (logic "1" or "0" at the output) depends on the state of the PD signal, controlled by the core logic (user design).

Immediately after the device is powered down, there would be some residual charge left on PMPOUT. If  $V_{CCI}$  is powered back up immediately while  $V_{CCA}$  is not powered, due to the residual charge, T3 may remain Off due to the residual charge. Therefore, the state of PDGATE (and consequently PDGATEB) is defined by the state of the latch, formed by T5 and T6. Since the core is not powered yet, the final state of the latch is unknown. For example, if T6 is On in the latch, PDGATEB will be in "High" state and T2 is On. Similarly, if PUGATEB happens to be in the Low state at the same time, a totem pole current will flow through T1 and T2, marked as  $I_T$  in Figure 2. The totem pole current on the I/Os is the source of the high inrush current during power cycling if  $V_{CCI}$  is powered before  $V_{CCA}$ . Since the configuration shown in Figure 2 is similar for both used and unused I/Os, the number of I/Os used in a design does NOT affect the value of the inrush current. The inrush current disappears once  $V_{CCA}$  is powered up to the functional level (~0.7 V) so the core is functional and the state of the T5–T6 latch is now defined.

This inrush current is affected by the amount of the residual charge left on the PMPOUT signal. If the residual voltage on PMPOUT falls below the threshold voltage of T3 ( $V_t$ ), this transistor will turn On and shut Off T1 and T2, causing the inrush current to drop. The residual charge on PMPOUT dissipates as leakage current. Therefore, the amount of the residual voltage on PMPOUT depends on the following:

- Temperature
- Time interval between power cycles
- Die size (the larger the die, the higher the leakage current)

Actel has conducted extensive tests to characterize the effects of the aforementioned parameters on the power cycling inrush current. The details of the test results are published in the *Actel RTSX-S Increased Inrush Current Phenomenon* paper, presented at 2003 MAPLD conference. The test results can be summarized as follows:

- The inrush current appears only when the RTSX-S devices are powered up immediately after power-down with  $V_{CCI}$  powering up first (Figure 1 on page 1).
- The inrush current does NOT pose any reliability concerns to the RTSX-S devices. A high current value raises electro-migration (EM) concerns. Actel EM calculation shows that the power cycling inrush current does not pose EM danger to the device reliability.
- The amount of inrush current during power cycling with improper sequence is lower in RT54SX72S devices than RT54SX32S devices. This is due to the die area of these devices. The RT54SX72S die is the largest in the family; therefore, the residual charge on PMPOUT dissipates faster due to a higher leakage current.
- The inrush current decreases as the operating temperature increases. This can be justified by the fact that leakage current of the die increases at higher temperatures, thereby discharging the PMPOUT signal faster.
- The inrush current decreases as the cycle delay/interval increases (Figure 1 on page 1). An extended cycle delay allows more residual charge to be dissipated. The test results show that at room temperature, the inrush current disappears if the cycle delay is on the order of tens of seconds.

## Power Cycling Recommendations and Solutions

Even though the inrush current does not affect the reliability of the RTSX-S devices, it is desirable to reduce or eliminate this current. From the test results summarized in the previous section, controlling the parameters affecting the inrush current, such as the cycle delay and temperature, helps to diminish the current value. However, as mentioned earlier, the inrush current phenomenon appears if and only if  $V_{CCI}$  is powered before  $V_{CCA}$  in power cycling. Hence, the definite solution to eliminate the inrush current phenomenon is to implement the correct power cycling sequence. An RTSX-S device does not require any particular power sequencing for initial power-up. In power cycling applications, Actel recommends power cycle profiles in which  $V_{CCI}$  is powered simultaneously with or after  $V_{CCA}$ .

The  $I_{CCI}$  inrush current phenomenon associated with the RTSX-S device family was corrected with the new UMC mask sets by forcing the internal charge pump to ground when either  $V_{CCI}$  or  $V_{CCA}$  is down.

As shown in Figure 3 on page 4, the inrush current was not observed in the RTSX-SU product family. This was verified for several worst-case power cycling conditions as listed in Figure 3 on page 4.

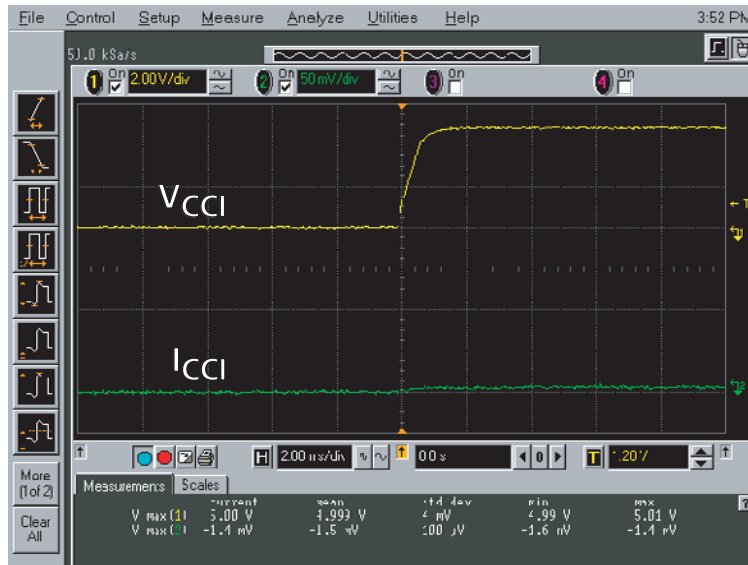


Figure 3 • No  $I_{CC1}$  is Observed When  $V_{CC1}$  is Powered Up Before  $V_{CCA}$  for RTSX-SU Devices

## Conclusion

The Actel RTSX-S family (RT54SX32S and RT54SX72S) does not require a particular power-up sequence. However, if the power-up/down occurs periodically (power cycling) with an improper power sequence profile and not enough delay between the cycles, an inrush current appears on  $I_{CC1}$  under specific conditions. The inrush current does not pose any reliability threat to the device. However, in order to reduce the cost of the power management circuitry of the board and to ensure the functionality of the board, Actel recommends a proper power cycling profile to eliminate the inrush current phenomenon. This application note emphasizes that the recommended requirements are only for power cycling applications. Initial power-up of RTSX-S devices does not require any particular sequence.

The RTSX-SU device family is equivalent to the RTSX-S device family, but has eliminated the inrush current phenomenon as discussed above.

## Related Documents

Actel RT54SX-S Particular Power Cycling Inrush Current Phenomena

[http://klabs.org/richcontent/MAPLDCon03/papers/p/p79\\_elftmann\\_p.pdf](http://klabs.org/richcontent/MAPLDCon03/papers/p/p79_elftmann_p.pdf)

Actel RTSX-S Increased Inrush Current Phenomenon

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## List of Changes

Previous Version	Changes in the current version 51900070-1/1.06	Page
51900070-0/3.04	The "Introduction" was updated.	1
	The "Power Cycling Recommendations and Solutions" section was updated.	3
	Figure 3 is new.	4

**Note:** The part number is located on the last page of the document.

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