RTAX-S/SL Clocking Resource and Implementation

Introduction

Actel's RTAX-S/SL FPGA family offers the most flexible global network scheme of any antifuse-based FPGA to date. This architecture provides eight segmentable chip-wide global networks, and dedicated power-on set/reset signals. This application note describes these global networks and the constraints used to segment them, discusses how to assign them in a design flow, and reviews design rules for input clock buffer assignment.

Architecture

Global Network Architecture Overview

All eight global networks in the RTAX-S/SL family can be accessed by either external or internal signals. Each family member has four types of global signals: HCLK, CLK, GCLR, and GPSET. Hardwired clock network (HCLK) drivers are all located on the north end of the die and are connected only to the clock input of each register cell (R-cell) and I/O register (Figure 1 on page 2). The hardwired HCLK networks have no antifuse connections between the clock drivers and register clock input pins. This allows minimal clock skew in HCLK networks. HCLK global networks are designed so that the clock skew is less than the shortest possible data path. Therefore, by design, HCLK networks are immune to hold-time violations. Note that if the HCLK network is segmented to route local clocks (refer to the "Clock Segmentation" section on page 8 for more details), the clock skew between different local segments may increase. This is usually due to a difference in clock insertion delays of the various local clock networks, as different routing is used to route the clock signal from the clock source to the entry point of various local clock networks. Hold violations on the network will be reported by Actel's SmartTime software as long as a constraint exists on the clocks being analyzed.

As shown in Figure 1 on page 2, the outputs of the four HCLK clock drivers (at the north end of the die) connect directly to the center of each core tile. From the center of each core tile, the HCLK network spreads horizontally across the core tile and then, through a set of smaller drivers, reaches all R-cells in that core tile via a column-based architecture.

Routed clock network (CLK) drivers are located on the south end of the device and can drive the CLK, PRE, CLR, and EN pins of registers, as well as any C-cell input. As shown in Figure 1 on page 2 (and like the HCLK network), the outputs of the CLK network drivers connect to the center of each core tile. The CLK networks spread vertically across the core tile and from there are distributed in horizontal rows to reach all logic and register cells of the tile. Also, as illustrated in Figure 1 on page 2, the horizontal rows of the CLK network inside the core tile are driven by two drivers, each driver covering half of the row (a half-row). The CLK network also offers a low-skew routing resource for clocks or any other skew-sensitive signals. However, as opposed to the HCLK networks, CLK networks are not hardwired. Therefore, the amount of skew on a CLK network varies with the distribution of the loads on the network. If the CLK network load on each half-row does not exceed 16 (including R-cells or C-cells), the CLK network will be immune to hold-time violations. Actel's Designer place-and-route software enforces the CLK half-row loading limit of 16. Like the HCLK network, if the CLK network is segmented to route local clocks (refer to the "Clock Segmentation" section on page 8 for more details), the clock skew between different local segments may increase due to a difference in the clock insertion delays of the various local clock networks. Hold violations on the network will be reported by Actel's SmartTime software as long as a constraint exists on the clocks being analyzed.

The global clear (GCLR) and global preset (GPSET) signals can drive the clear and preset inputs of each R-cell and I/O register on a chip-wide basis at power-up.

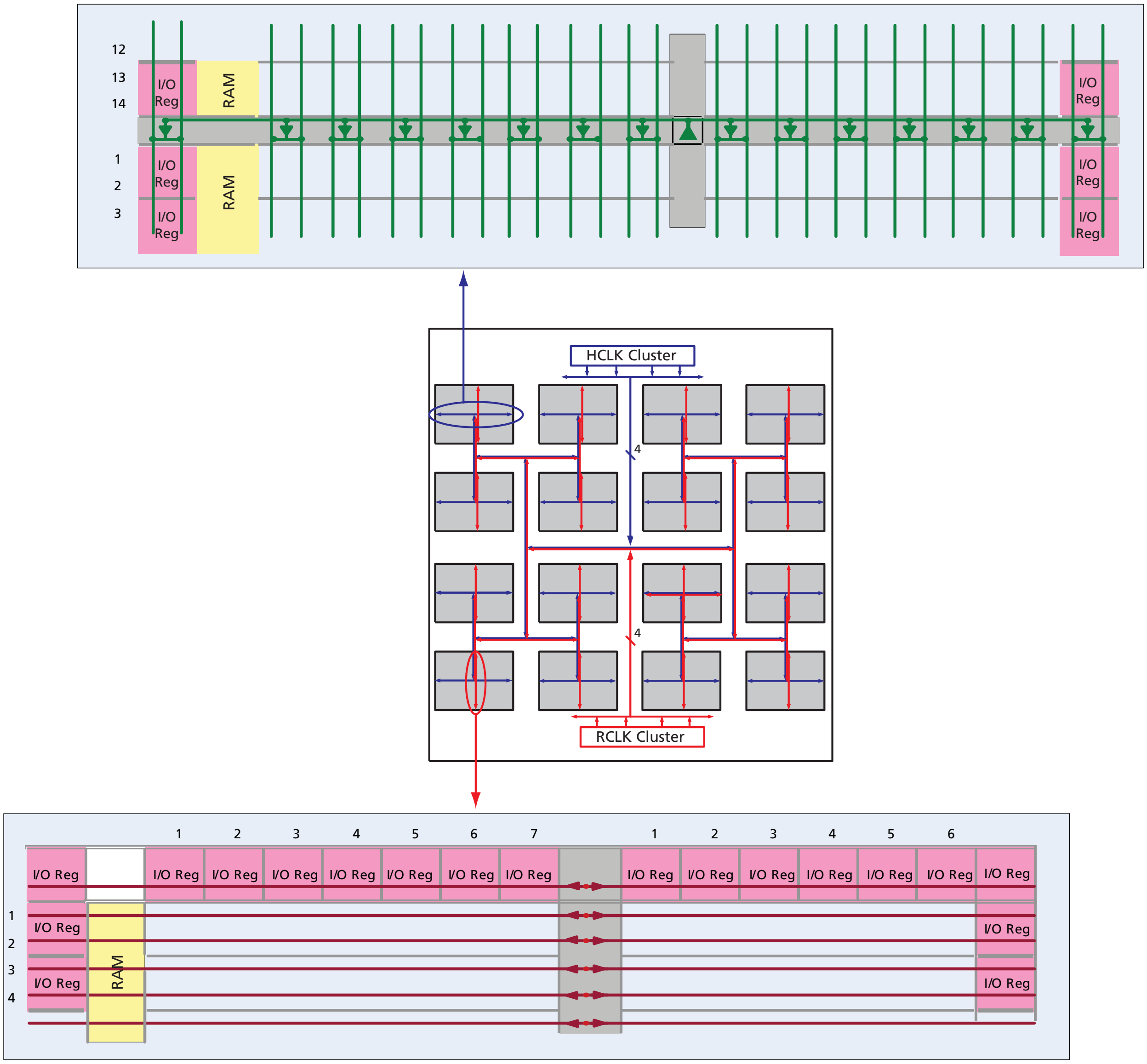

Figure 1 • **HCLK and CLK Network Architecture in RTAX-S/SL Devices**

CLK and HCLK Global Network Drivers

The global networks offer the flexibility to be driven by different types of sources, such as external pins or internal nets. This is made possible by the multiplexer architecture shown in Figure 2. For an external signal to directly drive a global network, it must first pass through an input buffer macro, which defines the I/O standard and voltage for that signal. The output of the input buffer macro is then driven to the clock network driver through a series of MUXes. In the case of an internal signal intended to drive a clock network, the signal is fed automatically to an internal buffer called CLKINT_W before it passes to the MUXes and the clock driver.

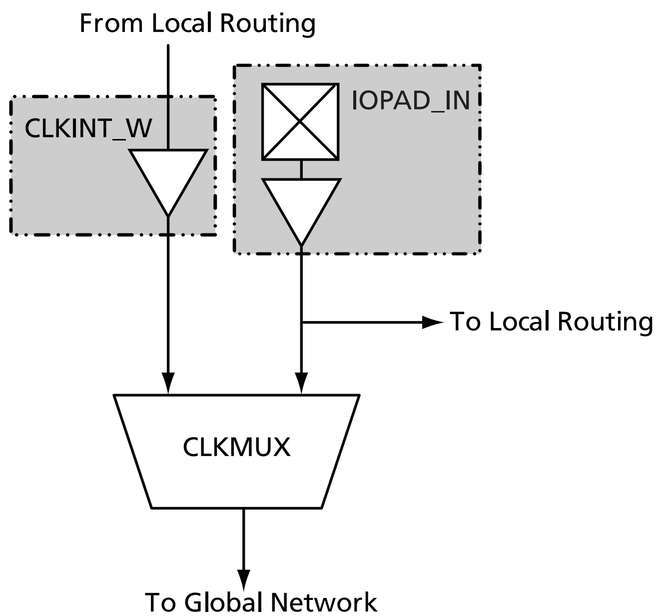

Figure 2 • **MUX Architecture of Global Clock Network Drivers**

Global Network Connections

An input MUX to each R-Cell determines whether the clock input of the register will be driven by HCLK, CLK, or some other signal. The HCLK network is hardwired to the inputs of these MUXes, eliminating the need for any antifuse connections within the network. The HCLK networks are also directly connected to the clock pin of I/O registers and embedded RAM/FIFO blocks in the device. HCLK cannot drive any other pins on any other modules. Note that HCLK networks can only drive the I/O register clock pins of I/O macros. For example, if a signal assigned to an HCLK network is to drive a chip output, it should be routed to an output buffer before the signal enters the HCLK network. Therefore, if the clock source is an input to the chip, it should be brought into the device through an input buffer (INBUF) and then enter the HCLK network via the HCLKINT macro, as shown in Figure 3. When schemes like this are used to connect signals to an HCLK network and other parts of the design (such as output buffers), designers should account for the timing skew between signals on the HCLK network and signals connected to other modules. The timing skew and other timing information can be derived from Actel's SmartTime software after completion of place-and-route.

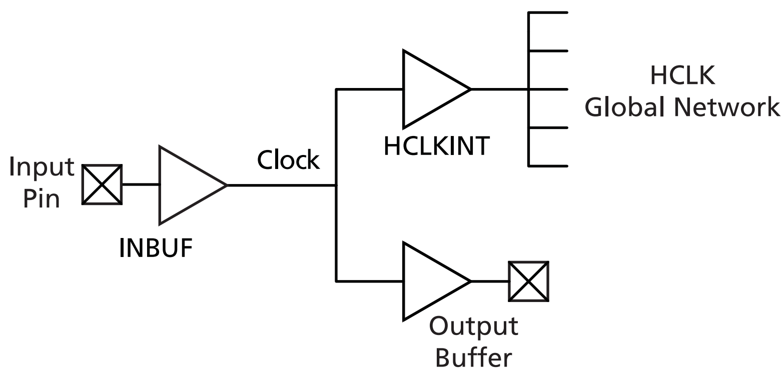

Figure 3 • **Clock Signal Driving I/O and HCLK Network**

The CLK networks offer the advantage of flexibility in that they can connect to a wide variety of module pins on RTAX-S/SL devices. They can connect to CLK, PRE, CLR, and EN pins of registers, and any input on C-cells. However, they cannot directly connect to data input pins on R-cells, such as D, A, B, or S. If a CLK network is connected to one of the aforementioned pins in the user's design, Actel's Designer software automatically inserts a buffer between the CLK network and the pin it needs to drive, and issues a warning during compile to notify the user of the buffer insertion.

Design Flow Considerations

Assigning Global Networks to I/O Banks

Global signal assignment to I/O banks is no different from regular I/O assignment, with the exception of the dedicated clock input pins. Determination of how to place global clock inputs can be simplified if the guidelines below are followed:

1. Only global signals compatible with both V_{CCI} and V_{REF} on an I/O bank can be assigned to the clock pins of that bank. Table 1 on page 5 lists global macros that are compatible with each other.
2. There is a pair of pins associated with each global input (P and N) to allow for differential signaling. Designers using a Physical Design Constraint (PDC) file for pin assignment must ensure that the P and N pins of the same pair are used for a differential clock input.

For single-ended inputs, the signal must be assigned to the P pad of the clock input. In such cases, the N pad will be available as a user I/O.

Table 1 • **Legal I/O Usage Matrix**

I/O Standard	LVTTL 3.3 V	LVCMOS 2.5 V	LVCMOS 1.8 V	LVCMOS 1.5 V (JESD8-11)	3.3 V PCI	GTL + (3.3 V)	GTL + (2.5 V)	HSTL Class I (1.5 V)	SSTL2 Class I and II (2.5 V)	SSTL3 Class I and II (3.3 V)	LVDS (2.5 V ± 5%)	LVPECL (3.3 V)
LVTTL 3.3 V (V_{REF} = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVTTL 3.3 V (V_{REF} = 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVCMOS 2.5 V (V_{REF} = 1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVCMOS 2.5 V (V_{REF} = 1.25 V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVCMOS 1.8 V	–	–	✓	–	–	–	–	–	–	–	–	–
LVCMOS1.5 V (V_{REF} = 1.75 V) (JESD8-11)	–	–	–	✓	–	–	–	✓	–	–	–	–
3.3 V PCI (V_{REF} = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
3.3 V PCI (V_{REF} = 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
GTL+ (3.3 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
GTL+ (2.5 V)	–	✓	–	–	–	–	✓	–	–	–	–	–
HSTL Class I	–	–	–	✓	–	–	–	✓	–	–	–	–
SSTL2 Class I & II	–	✓	–	–	–	–	–	–	✓	–	✓	–
SSTL3 Class I & II	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVDS (V_{REF} = 1.0 V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVDS (V_{REF} = 1.25 V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVPECL (V_{REF} = 1.0 V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVPECL (V_{REF} = 1.5 V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓

Notes:

1. *Note that GTL+2.5 V is not supported across the full military temperature range.*
2. *A "✓" indicates whether standards can be used within a bank at the same time.*
   Examples:
   a) LVTTL can be used with 3.3 V PCI and GTL+ (3.3 V) when V_{REF} = 1.0 V (GTL+ requirement).
   b) LVTTL can be used with 3.3 V PCI and SSTL3 Class I and II when V_{REF} = 1.5 V (SSTL3 requirement).
   c) LVDS V_{CCI} = 2.5 V ± 5%.

Implementing Global Macros in Schematic Designs

Adding global network buffers in schematics for RTAX-S/SL is no different from any other device family. Refer to the *Actel Libero Integrated Design Environment (IDE) User's Guide* (or online help) and *Antifuse Macro Library Guide*.

Implementing Global Macros in HDL Design Flow

In pure behavioral code, the synthesis tool libraries only infer the default global network macros, such as CLKBUF, CLKINT, and HCLKBUF. If no other constraints are applied, the default macros will be mapped to the default I/O standard set in Designer (similar to the mapping for INBUF mentioned above). However, given that the I/O banks to which these clock input buffers are assigned are compatible with the designated standard, the I/O standard of the default clock buffers can be changed using any of the following methods:

- Defining the I/O standard of clock inputs using PDC files
- Defining the I/O standard in the I/O attribute editor of Actel Designer's MultiView Navigator (MVN)
- Instantiating the specific I/O standard directly in the HDL code

The following are a few examples of global macro instantiations with a specific I/O standard:

CLKBUF_LVCMOS25 Driver

VHDL

```
component clkbuf_lvcmos25
port (pad  : in std_logic;
      y    : out std_logic);
end component
begin
-- concurrent statements
u2 : clkbuf_lvcmos25 port map (pad => ext_clk, y => int_clk);
end
```

Verilog

```
module design (______);
input _____;
output ______;
clkbuf_lvcmos25 u2 (
    .y(int_clk),
    .pad(ext_clk));
endmodule
```

HCLKBUF_LVDS Driver

VHDL

```
component hclkbuf_lvds
port (padp, padn  : in std_logic;
      y           : out std_logic);
end component
begin
-- concurrent statements
u2 : hclkbuf_lvds port map (
    padp => ext_clk_p,
    padn => ext_clk_n,
    y => int_clk);
end
```

Verilog

```
module design (______);
input _____;
output ______;
hclkbuf_lvds u2 (
    .y(int_clk),
    .padp(ext_clk_p),
    .padn(ext_clk_n));
endmodule
```

Inferring Clock Buffers in Synthesis

In pure behavioral HDL code, Synplicity® Synplify® will automatically try to detect clock inputs, generated clocks, or high-fanout nets and promote them to global clock networks using CLKINT, CLKBUF, or HCLKBUF macros. Designers can control the promotion of the signals to clock networks in Synplify by applying appropriate constraints (attributes). To prevent a signal from being promoted to a global clock network, the `syn_noclockbuf` attribute can be applied to the signal.

Local Clocks in Synthesis

Assigning local clocks to available low-skew clock network resources will be discussed later in this document. However, if a signal intended to be a local clock is run through synthesis, Synplify may buffer the signal because of high fanout. The fanout buffering is not needed once the signal is promoted to a local clock. However, Designer will not remove the buffers. Therefore, users need to prevent buffer insertion during synthesis. This can be done by setting a `syn_maxfan` constraint in Synplify to ensure that the buffering does not occur for the signals intended for local clock assignment.

Unused Global Input Pins

When global pins (designated as CLK or HCLK inputs) are not used as clock inputs, they can be used as regular I/Os. Actel's Designer software will automatically configure any unused I/Os as tristated outputs. Therefore, Actel recommends that unused HCLK input pins be tied to ground and that unused CLK inputs be connected to a known logic state (GND or V_{CCI}). If a single-ended signal is assigned to a global pin, the associated N pad is available to be employed as a user I/O. If not used, this N pad can be left floating.

Using the Dedicated Clear/Preset Networks

By default, all flip-flops in the RTAX-S/SL family will power up in the Reset state (logic 0) due to the hardwired power-on reset circuitry, via the GCLR network. This feature is built into the device and cannot be controlled by the user. However, Actel has implemented an option to power up the device with flip-flops in the Set state (logic 1) instead of the Reset state, via the GPSET network. This can be accomplished by choosing to program the GPSET Fuse in the Generate Programming File window when "Fuse" is selected in Designer. In addition to these built-in networks, a user-defined global clear/preset network can be designed to control reset of flip-flops during normal operation. This network can be driven by one of the CLK networks or by local routing resources.

Clock Segmentation

The RTAX-S/SL global clock networks can be segmented into smaller local networks. This is particularly beneficial for designs that have many small clock networks. As mentioned earlier, RTAX-S/SL devices have eight global clock networks (four HCLK and four CLK networks). Therefore, up to eight segmented local clocks can be assigned to the same region. For example, up to eight local clocks can be assigned to the same user-defined region (e.g., a designated core tile), or up to four local clocks can use the CLK resources in a row or group of rows.

The HCLK and CLK segmentation can be done with PDC files. A PDC file is used for establishing these and other physical (placement and routing) constraints. The PDC file should be imported in Actel's Designer software, along with the netlist, as a source file because the compiler needs to legalize the netlist and insert and/or delete buffers. There is a single PDC command to perform clock network segmentation:

> `assign_local_clock` – Assigns user-defined nets to local clock routing and constrains the placement of all loads for the given net to the specified region.

Row/Column Architecture

RTAX-S/SL devices use a tiled architecture; the number of core tiles varies with die size. Each core tile contains a number of logic SuperClusters, RAM blocks, and I/O cells (for tiles adjoining the I/O ring). As listed in Table 2 on page 14, the SuperCluster count is 336 per tile for all devices except the RTAX250S/SL, which has 176 SuperClusters per tile. The SuperClusters are arranged in rows and columns within a tile; the row and column counts are 28 and 12, respectively, for all devices except the RTAX250S/SL. Figure 4 on page 10 illustrates the tile arrangement for the RTAX1000S/SL device and shows a SuperCluster row and column of one tile. As discussed in the "Architecture" section on page 1, inside a given core tile, the CLK global network is distributed among SuperClusters on a row-by-row basis. In contrast, the HCLK network distribution in the core tile is on a column-by-column basis.

Note that, in the AX architecture, the HCLK columns drive all clusters in the column, but in the RTAX-S/SL architecture, the columns drive SuperClusters (SuperClusters consist of two clusters). In other words, in the AX architecture, the clusters in a SuperCluster are driven by two separate HCLK columns, which can be carrying two different clocks. On the other hand, the clusters in an RTAX-S/SL SuperCluster cannot be driven by two different local clocks (routed through HCLK network columns). Consequently, the number of columns available for local clocks in an RTAX-S/SL core tile is half of those for an AX core tile. This is important when Axcelerator® devices are used to prototype RTAX-S/SL designs. While designing local clocks in Axcelerator devices to prototype RTAX-S/SL devices, users should ensure that the clusters in a given SuperCluster are driven by the same clock.

Furthermore, as described in the "Local Clocks in Synthesis" section on page 7, users need to ensure that the signals intended to be local clocks do not have a fanout buffer tree, as these buffers will not be eliminated by promoting the signal to a local clock.

In the `assign_local_clock` command, the tile, rows, or columns assigned to the particular clock signal should be identified. With *M* columns and *N* rows in a particular tile, Figure 5 on page 10 shows the row/column labeling scheme used for the clock segmentation commands. In addition, the figure illustrates the identification of sample rows and columns. Understanding this nomenclature is critical in identifying the local clock region used in the `assign_local_clock` command.

The numerical indices of the rows and columns within each core tile are of great importance if the local clock network is subdivided inside the tile into smaller local networks. The row and column numerical indices within a tile include the RAM blocks and user I/Os of that tile (if the tile includes I/Os). For example, since the RAM blocks are on the left side of each tile (refer to Figure 4 on page 10), the first two columns of each tile are reserved for local clock routing to RAM blocks. However, these are not necessarily always columns 0 and 1. If a tile borders I/Os to its left, there are two additional columns to index the I/O tiles, and therefore, the clock routing columns reaching the RAM blocks are indexed as columns 2 and 3. Similarly, if I/Os border a tile on the north or south side, there are two additional local clock routing rows to I/O cells. As an example, the row/column counts and the numbering of these special rows and columns for the RTAX1000S/SL die are indicated for each tile in Figure 6 on page 11. The row/column numbering methodology for RTAX1000S/SL, described in Figure 6 on page 11, can be applied to other devices in the RTAX-S/SL family. Center tiles that do not border I/O tiles follow the same indexing as the RTAX1000S/SL central tile. For tiles that border I/Os, row/column indexing similar to that shown in Figure 6 on page 11 is applied—i.e., the indexing depends on whether the I/Os are on the north, south, east, or west side of the tile.

Command Syntax and Usage

assign_local_clock

The `assign_local_clock` command assigns user-defined nets to unoccupied local clock routing.

Syntax

```
assign_local_clock -type routing_resource_type -net netname
[local_clock_region1] [local_clock_region2] [local_clock_region3]
```

where

`routing_resource_type` is either "hclk" or "rclk".

`netname` is the name of the net being assigned to the local clock.

`local_clock_region` is defined by one of the following:

Reserving an Entire Tile

`tile<Tile Row><Tile Column>` (used with either CLK or HCLK)

Reserving a Row or Column within a Tile

`tile<Tile Row><Tile Column>.Row<Number>` (used with CLK)

`tile<Tile Row><Tile Column>.Column<Number>` (used with HCLK)

The command syntax is not case-sensitive. The `<Tile Row><Tile Column>` format is the number-letter coordinate scheme introduced in the previous section; reference "2C" and "3B" in Figure 5 on page 10. The `<Number>` identifier is the appropriate row or column within a tile, depending on the type of the resource (rows for CLK and columns for HCLK). When assigning the entire core tile to a local clock network, there is no range capability in the command. Therefore, for example, reserving three contiguous horizontal or vertical core tiles requires three separate `local_clock_region` arguments.

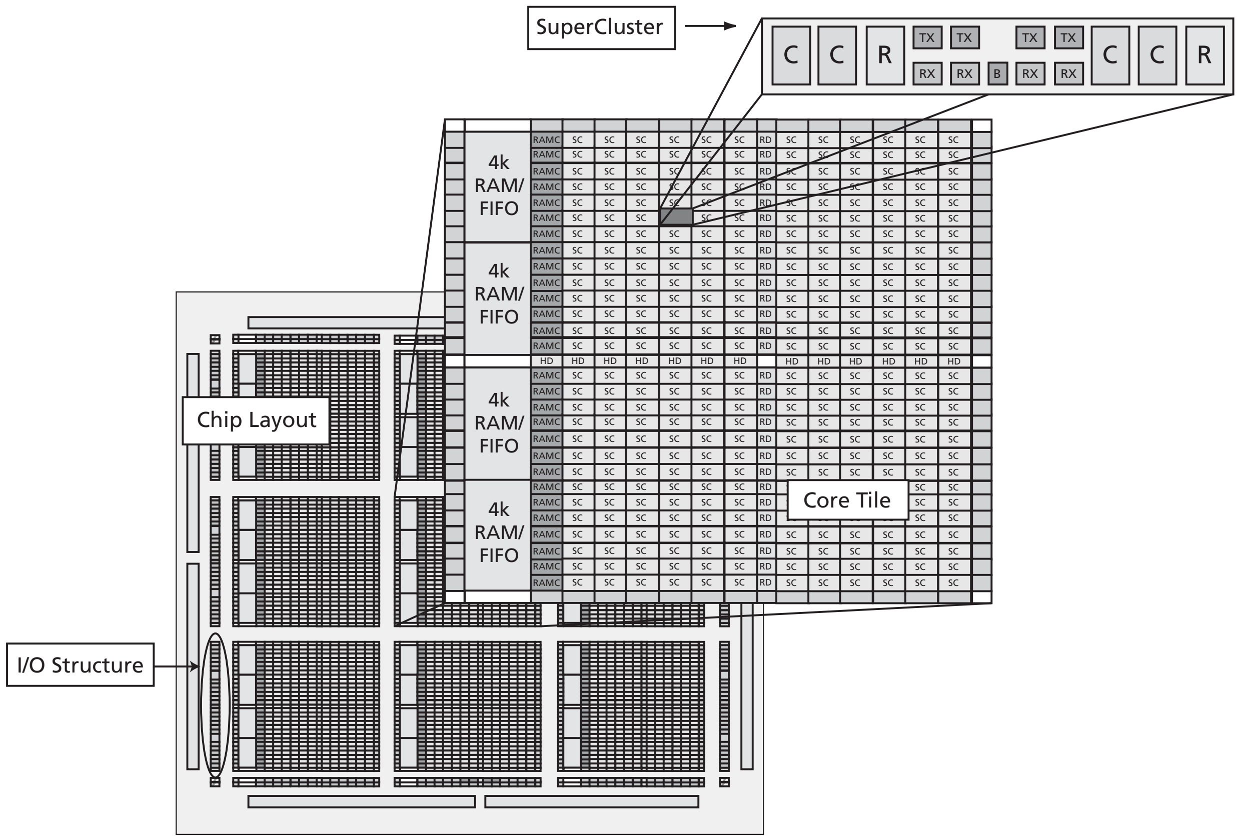

Figure 4 • **RTAX-S/SL Tile Organization**

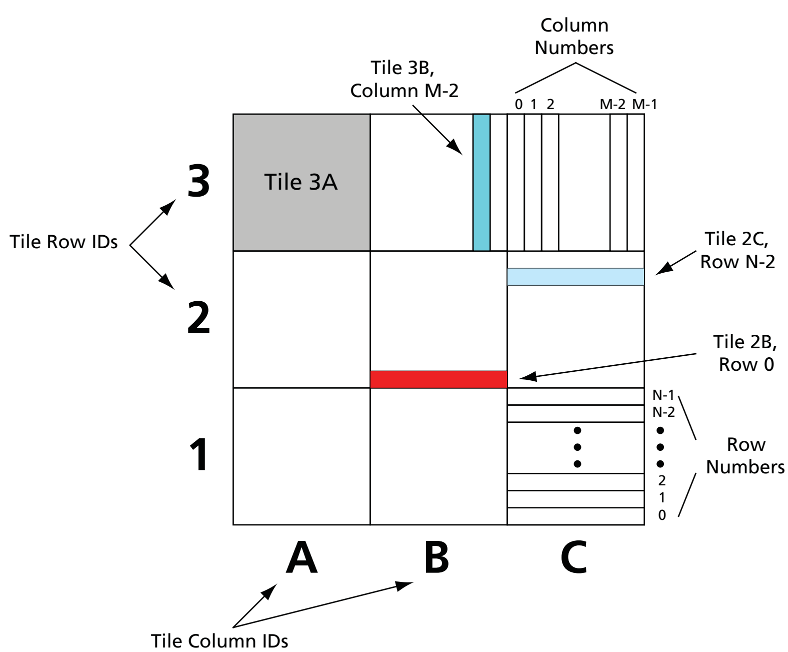

Figure 5 • **Row and Column Nomenclature**

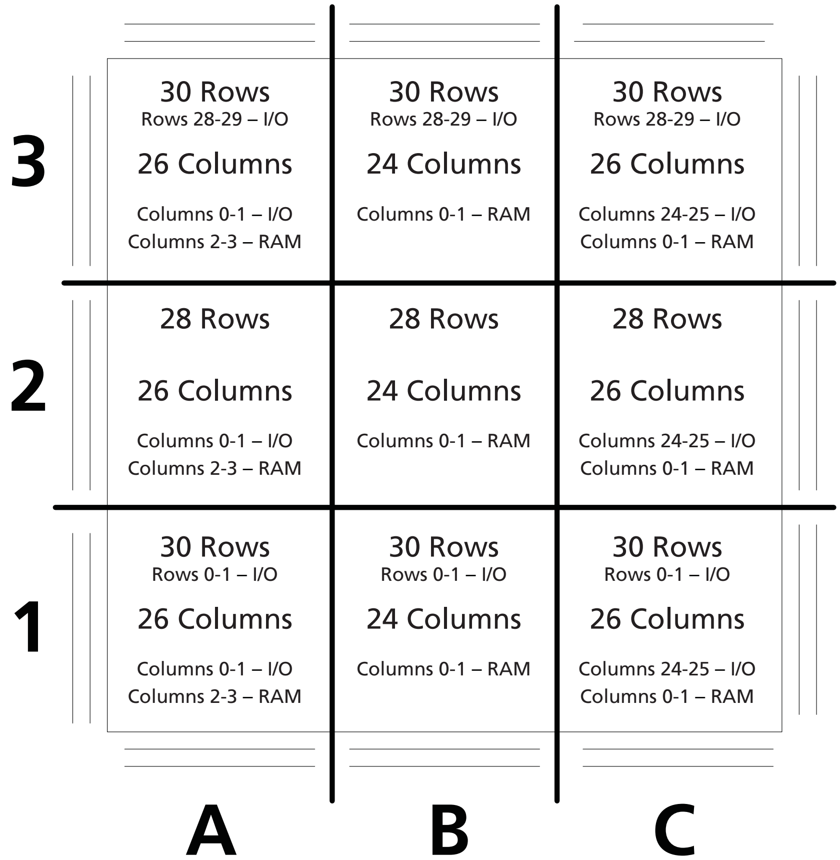

Figure 6 • **Row and Column Counts for Each Tile in RTAX1000S/SL**

When only assigning local clock networks to portions of a core tile, note that CLK resources only drive tile rows and HCLK resources only drive tile columns. Again, no range capability is provided. For example, when a local clock is assigned to three consecutive rows in a core tile, all three row indices should be specified in the `assign_local_clock` command. The following examples further elaborate on this.

Examples

Figure 7 illustrates several examples of the usage of the `assign_local_clock` command.

Example 1: Full Tile Assignment

Here the entirely of tile 3A is assigned to a local clock associated with net a1 using a CLK resource.

```
assign_local_clock -type rclk -net a1 tile3A
```

Example 2: Single-Column Assignment within a Tile

The following command assigns a single column in tile 2C to a local clock associated with net a2. The routing resource is an HCLK. The column is the next-to-last in an RTAX1000S/SL device—the 11th of 12.

```
assign_local_clock -type hclk -net a2 tile2C.col11
```

Example 3: Multiple-Column Assignment within a Tile

Here columns 0 through 4 of tile 2A are associated with a local clock on net a3. Note that the lack of ranging in the command syntax requires a separate argument for each column.

```
assign_local_clock -type hclk -net a3 tile2A.col0 tile2A.col1 tile2A.col2
tile2A.col3 tile2A.col4
```

Example 4: Assigning a Full Tile plus a Partial Tile

The following example shows a blend of different local clock region assignments. A complete tile, 1A, is assigned to a local HCLK associated with net a4. In addition, a single column of neighboring tile 1B is associated with the same local clock.

```
assign_local_clock -type hclk -net a4 tile1A tile1B.col0
```

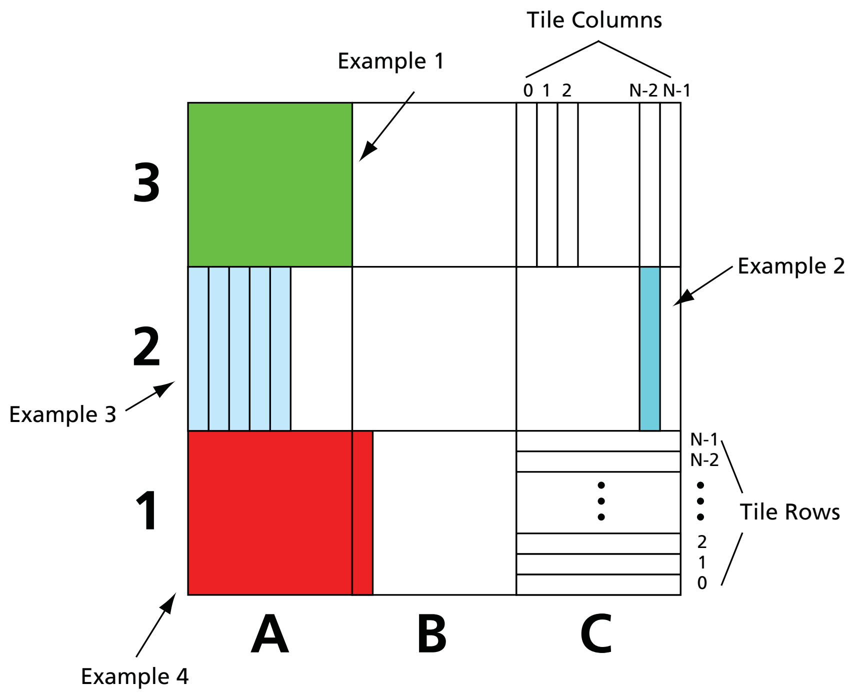

Figure 7 • **Illustrated Examples**

Special Considerations

Availability of Local Clock Networks

The signals already assigned to global clock networks in the netlist cannot be reassigned to local clocks. Furthermore, the global signals in the netlist take priority over local clocks; i.e., local clock assignment uses resources remaining after global assignments in the design netlist. In other words, assigned global resources are *not* demoted in favor of local clocks. However, local clocks can still be assigned even if all available global clock buffers (four HCLK and four CLK) are used to drive the clock networks. This requires users to apply some physical constraints on the loads of one or more global clocks.

Clock networks in the RTAX-S/SL architecture can be segmented with row (for CLK networks) or column (for HCLK networks) granularity. If the signal on the global clock, driving the global clock buffers, such as HCLKBUF or CLKINT, does not drive any loads on a particular row or column, that row or column will be available to be segmented from the global network and used for local clocks. The `assign_net_macros` constraint can be used to limit the span of a global signal to a certain region of the die.[1] Doing this will prevent the global signal from reaching into areas other than the designated region, therefore freeing the global resource in other regions of the die to be used for local clocks.

1. *Physical constraints, including* `assign_net_macros`*, are entered in a PDC file and imported along with the design netlist into Designer. For more information on the constraints and their syntax, refer to the Actel Design Constraints User's Guide or Designer online help.*

As an example, consider the following scenario: A design is targeting RTAX1000S/SL. All eight global clock buffers are driven by eight different clock inputs to the design. One of the global clock inputs, myCLK, is driving a CLKBUF. The output of the CLKBUF is a net with the global name of myCLK_c. The fanout of myCLK_c is limited to only 50 registers. In addition to the eight global clock inputs, there is another clock signal, myLocal_CLK, that drives a set of registers and needs to be assigned to a local clock network to avoid excessive skew. The following PDC commands limit the span of myCLK_c to tiles 1A, 1B, and 1C, and assign myLocal_CLK to tile 2A using global resources freed from the myCLK_c network:

```
define_region -name myCLK_region -type inclusive 0 0 809 29

assign_net_macros myCLK_region myCLK_c

assign_local_clock -type rclk -net myLocal_CLK tile2A
```

Local Clock Region Assignment Restriction for CLK Networks

In the RTAX-S/SL architecture, SuperCluster inputs are on both the top and bottom of each cluster (the signals can reach SuperCluster cells from both the top and bottom sides of the cell). When a row-based local clock is created using a CLK network, that local clock cannot reach the top inputs of the uppermost row of the local clock region. On the other hand, the layout tool does not allow a macro to be placed in a row unless both the upper and lower inputs of that row are reachable. For simplicity, this restriction applies even if no upper inputs are really needed in the region. In practice, this requires that all CLK regions have an extra row added on top of the intended local clock region. Therefore, the minimum size of a CLK local clock region is two rows. Furthermore, these extra rows can overlap. In other words, N rows in a tile can support up to N – 1 individual local clock networks.

Note that the above restriction does not apply if an entire core tile is assigned to a CLK-based local clock region unless the core tile is expected to be full or nearly so.

In contrast, there is NO similar restriction on columns in local HCLK-based clock networks. Therefore, M columns in a core tile can support up to M individual local HCLK networks.

Example 5: Adding an Extra Row for CLK Assignments

The following example (illustrated in Figure 8) assigns rows 0 to 2 of tile 2B to a local clock named a5. To address the above restriction, an extra row, row 3, is also assigned and is the top row of the group.

```
assign_local_clock -type rclk -net a5 tile2B.row0 tile2B.row1 tile2B.row2
tile2B.row3
```

Note that in the above example, the place-and-route tool will not assign any macros driven by local clock a5 to row 3 of tile 2B.

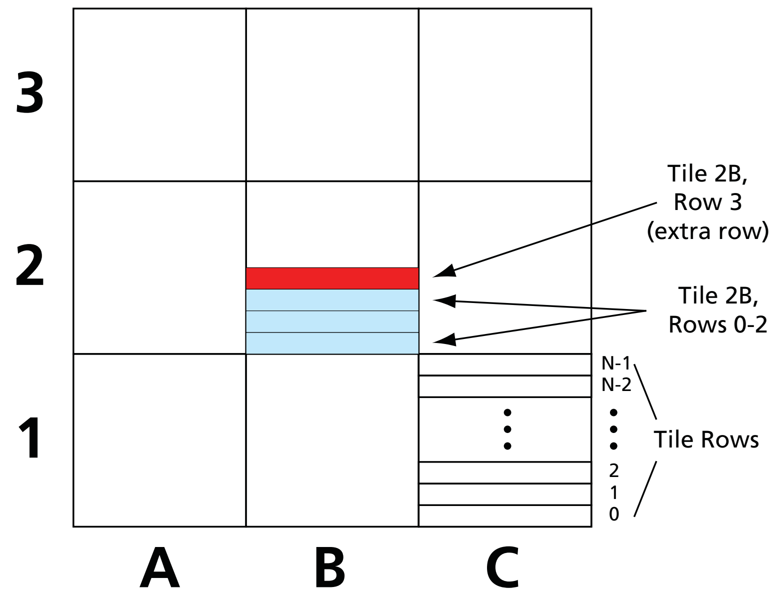

Figure 8 • **Extra Row Assignment for CLK Region**

Possible Numbers of Local Clock Segments

This section summarizes the maximum numbers of local CLK and HCLK segments for each member of the RTAX-S/SL family. To simplify the calculation, the segments associated with I/O rows and columns have been omitted.

The maximum numbers of CLK and HCLK segments are given by EQ 1 and EQ 2:

$$CLKmax = (M - 1) \times T$$

EQ 1

$$HCLKmax = N \times T$$

EQ 2

where

M = number of logic rows per tile, excluding I/O rows

N = number of cluster columns per tile, excluding I/O columns

T = number of tiles

Table 2 summarizes the totals for each member of the family.

Table 2 • **Maximum Numbers of HCLK and CLK Segments for RTAX-S/SL Family Members**

Device	Number of Tiles	SuperClusters per Tile	Logic Tiles		HCLK Segments	CLK Segments
			SuperCluster Columns	Rows		
RTAX250S/SL	4	176	24	16/8	64	92
RTAX1000S/SL	9	336	28	24/12	216	243
RTAX2000S/SL	16	336	28	24/12	384	432

Conclusion

The RTAX-S/SL family offers eight global clock networks and a global reset/preset capability. The architecture of global clock networks in RTAX-S/SL devices offers the flexibility of segmenting into smaller local clock networks. This improves the performance of designs in which there are relatively large numbers of clock signals with moderate fanouts. A given global routing resource can be subdivided into local clock regions to allow access to low-skew clock networks for all the clocks in the design.

Related Documents

User's Guides

Actel Libero Integrated Design Environment (IDE) User's Guide (or online help)

http://www.actel.com/documents/libero_ug.pdf

Antifuse Macro Library Guide

http://www.actel.com/documents/libguide_ug.pdf

Designer Constraints User's Guide

http://www.actel.com/documents/des_constraints_ug.pdf

List of Changes

Previous Version	Changes in the current version 51900166-2/11.07	Page
51900166-2/11.07	In the definitions for EQ 2, the definition for N was changed from row to column.	14
	In Table 2, the SuperClusters per Tile was updated for the RTAX2000S/SL device. It was changed from 33,616 to 336.	14
51900166-1/9.07	Figure 2 was updated to eliminate the PLL and focus on the actual RTAX-S/SL architecture.	3
51900166-0/8.07	In the "Global Network Architecture Overview" section, the half-row number was changed from 12 to 16.	1

Note: *The part number is located on the last page of the document.*

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