

Differences Between RTAX-S/SL and Axcelerator[®]

Introduction

RTAX-S/SL is Actel's latest FPGA family designed for space applications and is a derivative of the Actel Axcelerator FPGA family. The RTAX-S/SL architecture is based on Actel's multi-featured, high-density AX architecture but with enhancements for a high level of single-event upset (SEU) immunity. To achieve this, some Axcelerator features were removed from the silicon and other features were further enhanced.

The purpose of this application note is to facilitate the prototyping process by highlighting the differences between RTAX-S/SL and Axcelerator. This document supplements the Actel application note *Prototyping RTAX-S and RTAX-SL Devices*.

RTAX-S/SL Modifications for SEU Immunity

To ensure SEU immunity, the following Axcelerator features are NOT included in the RTAX-S/SL feature set.

PLL

All eight PLLs that are included in Axcelerator are NOT part of RTAX-S/SL. The corresponding PLL supply voltage pins (V_{CCPLX} and V_{COMPLX}) have become No Connects (NC). These pins are not connected to any circuitry in the device and can be driven to any voltage or left floating with no effect on the operation of the device. In addition, the special PLL macros cannot be used because they are not part of the RTAX-S/SL macro library. These include PLLINT, PLLRCLK, PLLHCLK, and PLLOUT.

PerPin FIFO and I/O FIFO Embedded Controller

All PerPin FIFOs and I/O FIFO Embedded Controllers included in Axcelerator are NOT part of RTAX-S/SL. Thus, the user cannot instantiate PerPin FIFO macros and I/O FIFO Embedded Controller macros in an RTAX-S/SL design, because these components are not part of the RTAX-S/SL macro library.

Low-Power (LP) Mode

The low-power mode capability that is featured in Axcelerator is NOT part of RTAX-S/SL. The corresponding LP pin has become a GND. However, the V_{PUMP} pin is still available for external charge pump access for chip power savings. When the external charge pump applies 3.3V to the V_{PUMP} pin, the internal charge pump is disabled, and the external charge pump will then drive the internal "pump" line. However, when the internal charge pump is used, the V_{PUMP} pin should be grounded.

Programmable Input Delay Elements

For Axcelerator, a programmable input delay element can be enabled for each clock input in addition to regular inputs. However, for RTAX-S/SL, these input delay elements are NOT available for clock inputs or regular inputs.

Enhancements for Improved SEU Immunity

As mentioned earlier, several Axcelerator features have been improved to enhance SEU immunity. The following sections describe those features and their improvements.

Flip-Flops

All dedicated flip-flops employ Triple Modular Redundancy (TMR). This includes all flip-flops implemented with R-Cells and all I/O registers: input registers (InReg), output registers (OutReg), and enable registers (EnReg).

Global Resources

All four hardwired clock (HCLK) and all four routed clock (CLK) clock-trees have been enhanced to improve SEU immunity.

Embedded SRAM/FIFO

Since the SRAM does not employ TMR, error detection and correction Intellectual Property (EDAC IP) can be implemented to enhance SEU immunity. For EDAC implementation details, see Actel's application note, [Using EDAC RAM for RadTolerant RTAX-S/SL and Axcelerator FPGAs](#). The internal RAM/FIFO controller is NOT RadTolerant but can be implemented at the user's discretion, based on system and/or SEU requirements. Alternatively, the SRAM can be controlled through the use of regular core logic.

JTAG/Probe Circuitry

The JTAG circuitry is not RadTolerant. Therefore, the TRST pin should be hardwired to ground during flight to hold the JTAG circuitry in reset. This ensures maximum SEU immunity. Note that the TRST pin has an optional 10k pull-up resistor that can be disabled.

During flight, the following configurations for all JTAG and Probe pins are recommended (Table 1).

Table 1 • JTAG and Probe Pin Recommendations for Flight

JTAG and Probe Pins	Configurations
TCK	<ul style="list-style-type: none"> Can be hardwired to V_{CCDA} or ground Can be driven to V_{CCDA} or ground Must not be left unterminated
TDO	Must be left unconnected
TDI	<ul style="list-style-type: none"> Can be hardwired or driven to V_{CCDA} Can be left unconnected (equipped with internal 10k pull-up resistor)
TMS	<ul style="list-style-type: none"> Can be hardwired or driven to V_{CCDA} Can be left unconnected (equipped with internal 10k pull-up resistor)
TRST	Must be hardwired to ground (equipped with optional internal 10k pull-up resistor)
PRA/B/C/D	Must be left unconnected

Additional Features

Packaging

Table 2 lists the planned package offerings for RTAX1000S and RTAX2000S.

Table 2 • Planned Package Offerings

Package	Device Package Pin Count	
	RTAX1000S	RTAX2000S
CCGA	624	624, 1152
CQFP	352	352

Note: Please contact your Actel sales representative for final package listing.

Development Software Support (Actel's Libero® Integrated Design Environment (IDE) and Designer software)

Because some designers may be accustomed to using certain Axcelerator features, Actel's Libero IDE tool suite and Actel's Designer software will produce error messages if these features are not supported in RTAX-S/SL. For example, the instantiation of unsupported macros (i.e., PerPin FIFO and PLL macros) will generate error messages.

Conclusion

In anticipation of the new RTAX-S/SL FPGA family offerings, many designers are creating designs using Axcelerator documentation. RTAX-S/SL and Axcelerator are quite similar in many ways; however, it is imperative that the designers take into consideration the RTAX-S/SL enhancements and restrictions and design accordingly.

Related Documents

Datasheets

RTAX-S RadTolerant FPGAs

http://www.actel.com/documents/RTAXS_DS.pdf

Axcelerator Family FPGAs

http://www.actel.com/documents/AX_DS.pdf

Application Notes

Prototyping RTAX-S and RTAX-SL Devices

http://www.actel.com/documents/PrototypingRTAXS_AN.pdf

Using EDAC RAM for RadTolerant RTAX-S/SL and Axcelerator FPGAs

http://www.actel.com/documents/EDAC_AN.pdf

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