

Storage Solution for PXA270 platform Users Guide v1.0

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1 Introduction

The daughterboard provides a means of adding IDE functionality to an XScale processor, using an Actel ProASIC3 FPGA for the IDE bridge logic. The board also incorporates connectors for additional interfaces for future reuse, and support for an embedded processor. This board is intended for sales demonstrations, not for resale.

1.1 Board Features

The board has the following interfaces:

- 2.5" HDD host connector
- Compact Flash host connector
- CE-ATA header/FPC socket
- IDE FPC socket (optional)
- PCMCIA/CardBus host connector
- Mini-PCI host connector
- Two SDIO host connectors
- Motherboard connectors
- Debug header
- Programming header
- Power Jack
- Test/probe points
- Oscillator/Oscillator socket
- CoreM7 JTAG ICE header
- DB-9 and RS-232 driver

Additionally, the board has the following components:

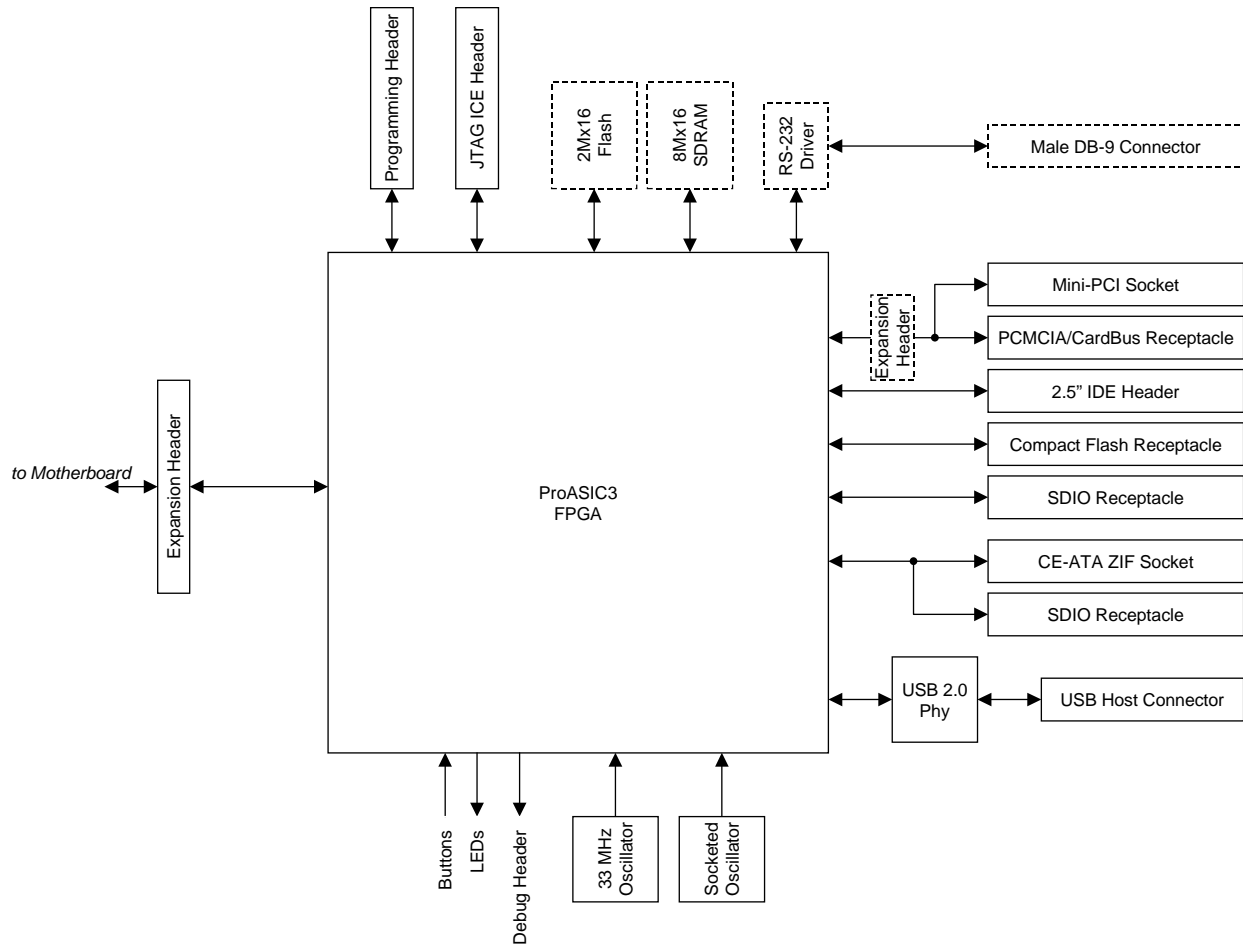
- ProASIC3E FPGA (A3PE600-FG484)
- 2M x 16-bit asynchronous SDRAM (20ns or faster)
- 256k x 16-bit or larger parallel NOR Flash
- Regulators from 5V to required voltages
- Power LED
- 4 user LEDs
- 1 user button
- 4-bit DIP switch
- 1 reset button and reset debounce/monitor chip
- System oscillator
- Auxiliary oscillator

2 General Description

The board contains a ProASIC3E A3PE600-FG484 FPGA for all functions. All connectors (except Mini PCI), buttons and switches are placed on the left, right or bottom edges of the board. An optional power jack is placed at the right rear corner of the board. The board supports mechanical mounting of a 1.8" or 2.5" hard drive; the hard drive must be mounted on standoffs and connected to the board with a cable.

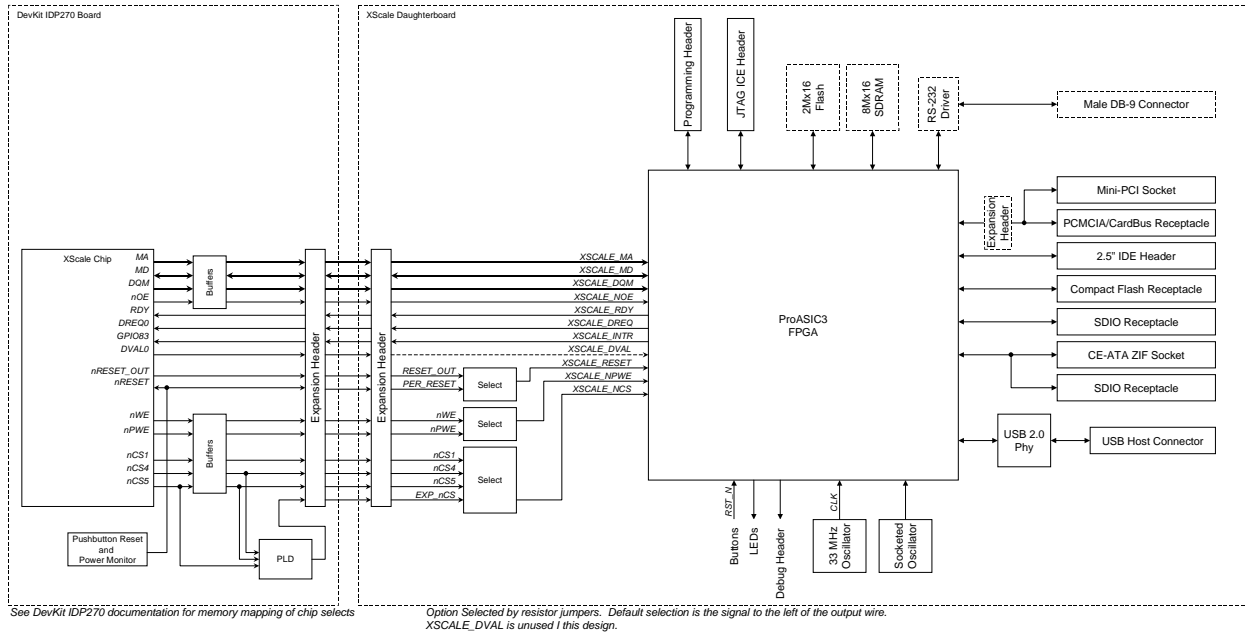
2.1 Board Block Diagram

The block diagram for the board is illustrated below.



2.2 System Block Diagram

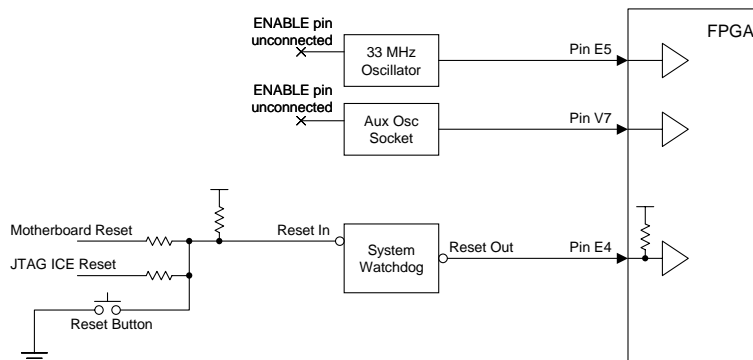
The block diagram for the board daughterboard plus motherboard is shown below.



The DevKit IDP270 motherboard contains the XScale processor, plus a PLD for peripheral functions. The motherboard expansion header is used to connect the ProASIC3 FPGA to the XScale. The expansion header on the motherboard connects all relevant signals from the XScale chip (directly or through a buffer) except EXP_HDR_nCS. EXP_HDR_nCS is generated inside the PLD, and is asserted when nCS3 is asserted and MA bit 24 is '1'. Refer to the IDP270 documentation for additional information.

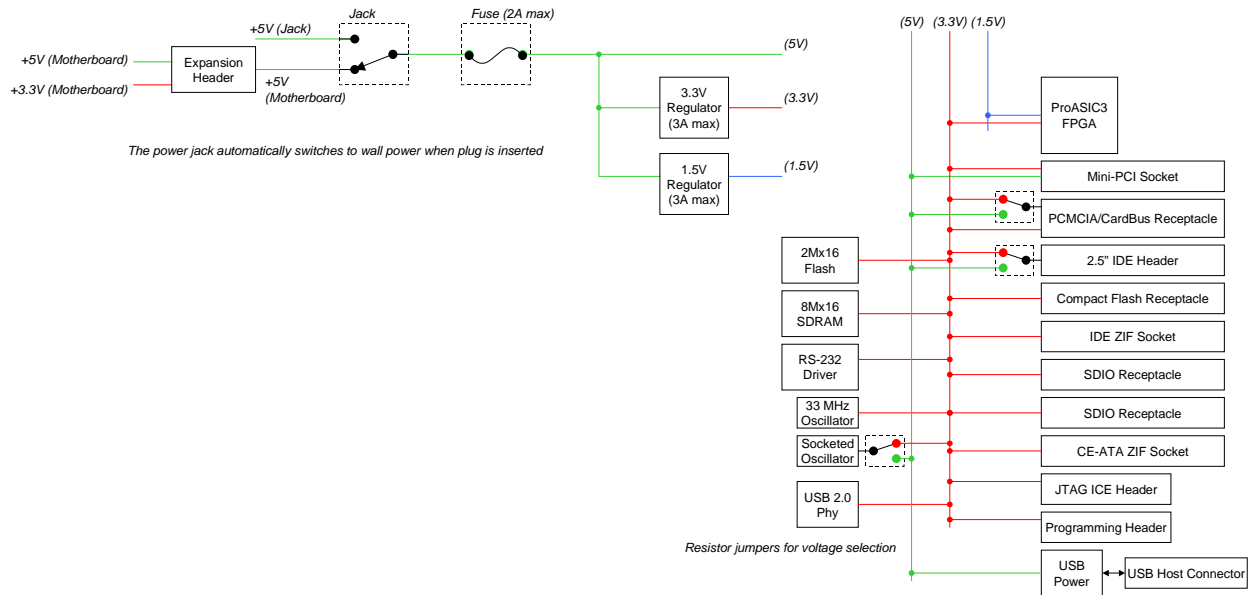
2.3 Clock Distribution

The clock distribution diagram is shown below.



2.4 Power Distribution

The power distribution on the board is shown below.



3 Interface Descriptions

The board supports a number of interfaces. These are described in this section.

3.1 Power Jack (CN1)

A barrel connector jack is provided for external power. The jack accepts a plug with a 2.5 mm center pin, and required +5V on the barrel and ground on the center pin. When no plug is inserted in the jack, the jack is configured to a route power from the motherboard. When the plug is inserted, the jack disconnects power from the motherboard connector.

3.2 Mini-PCI (CN2)

A Mini-PCI Type III receptacle is provided for addition of communication interface cards, such as 802.11. All Mini-PCI signals are connected directly to the FPGA, and are shared with the CardBus connector (CN3), and the secondary motherboard header (CN16). Note that some of the Mini-PCI signals are shared with GPIO functions; see Section 4.4, “GPIO Pin Multiplexing” for additional information.

3.3 PCMCIA/Cardbus (CN3)

A Cardbus allows the addition of PCMCIA and Cardbus (PC Card) devices to the board. All Cardbus signals are connected directly to the FPGA, and are shared with the Mini-PCI connector (CN2), and the secondary motherboard header (CN16). The Cardbus connector can be powered by 3.3V (by populating R12 with a zero-ohm resistor) or 5V (by populating R11 with a zero-ohm resistor). Note that some of the Cardbus signals are shared with GPIO functions; see Section 4.4, “GPIO Pin Multiplexing” for additional information.

3.4 FPC IDE (CN4)

The FPC (flexible printed circuit) IDE connector supports a 1.0” PATA disk drive with a 35-pin signal and power interface. A flex connector is required to attach a disk drive to this connector. Note that the FPGA connections to CN4 are shared with CN5 and CN6.

3.5 IDE (CN5)

The IDE interface supports a 2.5” disk drive, including the 40 IDE signal pins and the power pins. A 2.5” or 1.8” hard drive may be connected via standard 44-pin 2mm pitch ribbon cable. A 3.5” hard drive may be connected by attaching a 2.5”-to-3.5” hard drive adapter to the board, then attaching a 3.5” hard drive ribbon cable to the adapter. A 2.5” hard drive may be powered from the demo board. 2.5” drive power can be either 3.3V (a zero-ohm resistor populated at R42) or 5V (a zero-ohm resistor populated at R41). A 3.5” hard drive must be independently powered. Note that the FPGA connections to CN5 are shared with CN4 and CN6.

3.6 Compact Flash (CN6)

The Compact Flash connector supports Type I and Type II 3.3V Compact Flash cards. All Compact Flash pins are driven directly by the FPGA. Some of the pins are shared with GPIO functionality; see Section 4.4, “GPIO Pin Multiplexing” for additional information. Note that the FPGA connections to CN6 are shared with CN4 and CN5.

3.7 SDIO (CN7 and CN8)

Two independent MMC/SD/SDIO card receptacles are provided, with all signals connected directly to FPGA pins. Due to FPGA pinout restrictions, only the protocol signal pins are connected to the FPGA. The Card Detect and Write Protect pins are not connected; if these functions are required, they can be wired a pin on an unused connector, or to an unused pin on any other connector. Note that the CN8 signals are shared with the CE-ATA connector (CN9).

3.8 CE-ATA (CN9)

A 12-pin FPC connector is available for connection of a CE-ATA drive to the board. The CE-ATA signals are connected directly to the FPGA. Note that the CE-ATA signals are shared with the second SDIO connector (CN8).

3.9 USB (CN10)

A USB host connector is provided for interfacing to a USB device. The USB circuit includes a USB 2.0 high-speed capable Phy chip and USB power (VBUS). The USB Phy connects to the FPGA via an 8-bit UTMI interface. VBUS with overcurrent protection is enabled by default. VBUS power can also be controlled by the FPGA by adding a zero-ohm resistor to the R76 pads. See also Section 4.4, “GPIO Pin Multiplexing”.

3.10 Motherboard Connectors (CN11 and CN16)

Two motherboard connectors are provided: a primary connector and a secondary connector. Both connectors are 100-pin dual 0.05-inch sockets. The primary connector is dedicated for connection to a motherboard; the secondary connector is shared with the Cardbus (CN3) and Mini-PCI (CN2) connectors. The primary connector pinout mates directly to the BSquire DevKit IDP270 motherboard; the secondary connector has a general purpose pin assignment. Both connectors interface to the FPGA. Power can be provided to the board via the primary connector. The secondary connector is tied to the power output (after the fuse) and can be used to provide power to a motherboard if desired. Note that some of the motherboard address pins are shared with the Flash address pins. See Section 4.4, “GPIO Pin Multiplexing” for additional information.

3.11 JTAG ICE (CN12)

A 20-pin ARM JTAG ICE connector is provided to easily facilitate the implementation of the CoreM7 processor in the FPGA. If another processor is implemented in the FPGA, this interface could be used for the JTAG ICE by creating a custom adapter. Note that the Debug Request and Debug Acknowledge pins are shared with GPIO; see Section 4.4, “GPIO Pin Multiplexing” for additional information.

3.12 RS-232 (CN13)

A DB-9 RS-232 circuit is provide for general purpose serial communication (such as a debug console). The RS-232 circuit implements TX and RX communication with loopback flow control.

3.13 Programming Header (CN14)

The FPGA programming header is available for programming the FPGA. It is configured with VPUMP and VJTAG connected directly to 3.3V.

3.14 GPIO Header (CN15)

Sixteen GPIO pins are available for user-defined functions (such as debug or a front-panel interface). The GPIO header included the 16 GPIO pins, driven directly by the FPGA, plus 5V, 3.3V and ground connections. All GPIO functions are shared with other optional features; see Section 4.4, “GPIO Pin Multiplexing” for additional information.

3.15 LEDs (D1 and D3-D6)

A 5V power LED lights when power is applied to the board. This LED is powered directly from the power source, and is not an indicator of power good (voltage within prescribed range), but as an indicator that power is applied. In addition, four LEDs are available to be used as status indicators, or for debug.

3.16 Fuse (F1)

A 2A fast-acting TR-5 Fuse is provided with the board, socketed in a fused holder. Board power consumption can be measured by replacing the fuse with a current meter.

3.17 Buttons (SW1 and SW2)

A reset pushbutton is provided to serve as a hard reset (SW1), and a general purpose pushbutton is provided for user-defined functions (SW2). The reset button is debounced with a system monitor chip; this chip also provides a reset output if the board voltage drops below 4.5V. The user pushbutton is not debounced, and may be debounced by logic in the FPGA if desired. Both buttons are active low, with 10 kOhm pullup resistors.

3.18 DIP Switch (SW3)

A four-bit DIP switch allows for configuration settings. Three of the DIP switches are connected directly to the FPGA; the fourth switch is available to be wired to any unused pin, if needed. All DIP switches are active low.

4 Configuration Options

4.1 Motherboard Signal Selection

Several pin connection options are available on the daughterboard, and are selected by adding a zero-ohm resistor to the path to be connected. These selection options are shown above, and are defined in the table below.

Function	Resistor	Selection	Default
Reset	R96	nRESET_OUT	✓
	R95	nRESET	
Chip select	R90	EXP_HDR_nCS	✓
	R91	nCS1	
	R88	nCS4	
	R89	nCS5	
Write enable	R92	nWE	
	R93	nPWE	✓

The board has a dedicated reset button, SW1, in addition to the reset from the motherboard, and its own clock source; the daughterboard runs asynchronous to the motherboard board.

4.2 Interface Voltage Selection

Interfaces that can accept devices with more than one voltage option use resistor jumpers to select the interface voltage. These are given below.

Interface	Resistor	Voltage	Default
Oscillator (Y2)	R129	3.3V	✓
	R130	5V	
PCMCIA/Cardbus (CN3)	R12	3.3V	✓
	R11	5V	
2.5" HDD (CN5)	R42	3.3V	✓
	R41	5V	

4.3 Other Function Selects

Other interface function selects are given below.

Interface	Resistor	Voltage	Default
Cardbus interrupt (CN3)	R38	INTA	✓
	R39	INTB	✓

4.4 GPIO Pin Multiplexing

Due to the number of available FPGA user I/O pins, some functions are multiplexed. That is, they are used for more than one independent function. The table below indicates the multiplexed signals.

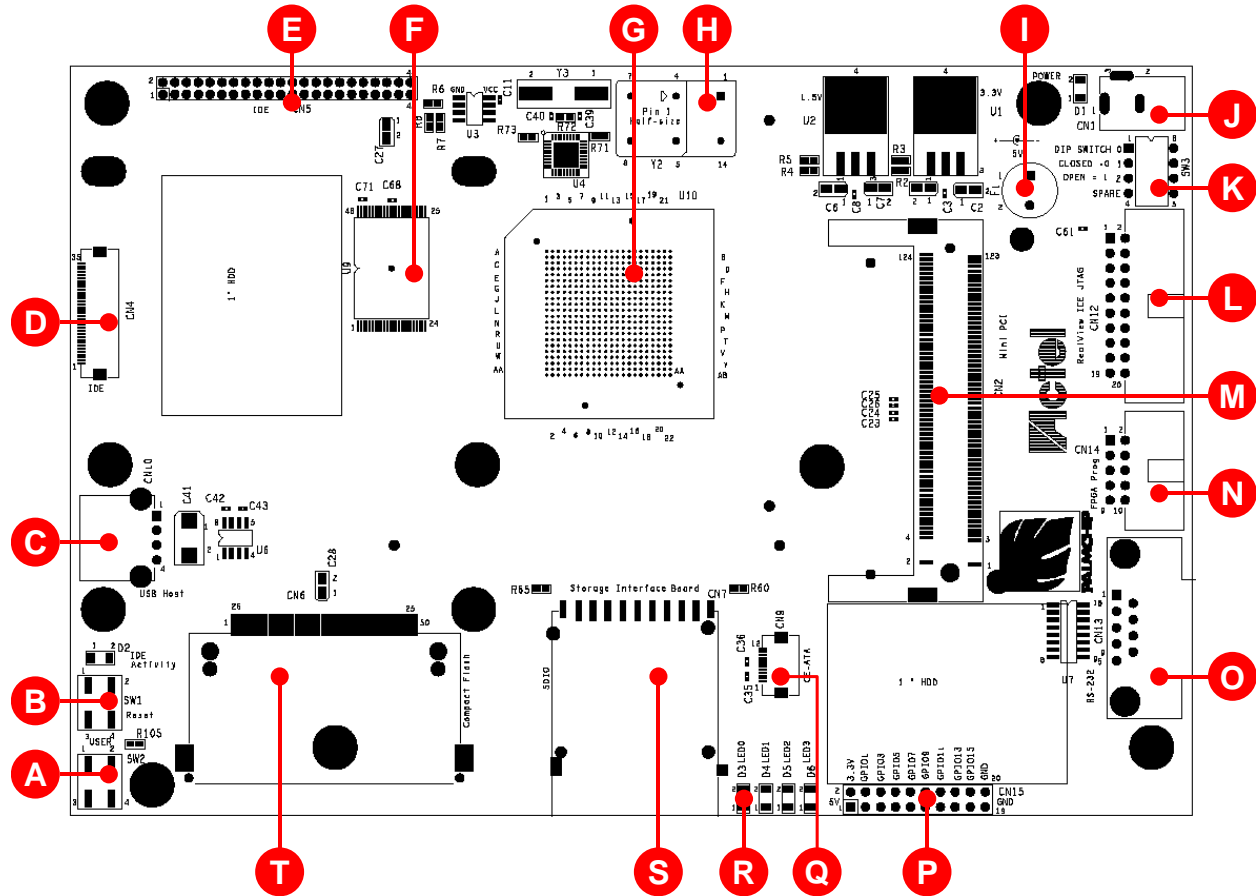
Function 1	Function 2	Function 2 Enabled

GPIO 0	IDE CSEL	No
GPIO 1	Board Power Enable	No
GPIO 2	USB VBUS Power Enable	No
GPIO 3	USB VBUS Overcurrent	No
GPIO 4	ARM JTAG ICE DBGREQ	No
GPIO 5	ARM JTAG ICE DBGACK	No
GPIO 6	Mini PCI PME	Yes
GPIO 7	Mini PCI M66EN	Yes
GPIO 8	Cardbus CD1	Yes
GPIO 9	Cardbus CD2	Yes
GPIO 10	Cardbus VS1	Yes
GPIO 11	Cardbus VS2	Yes
GPIO 12	Compact Flash CD1	Yes
GPIO 13	Compact Flash CD2	Yes
GPIO 14	Compact Flash VS1	Yes
GPIO 15	Compact Flash VS2	Yes
Memory Address[20:12]	XScale VLIO Address[18:10]	Yes

All GPIO pins are brought out to the GPIO header. Secondary functions for GPIO pins are connected via zero-ohm resistors; resistors for GPIO 0-5 secondary functions are not populated by default. GPIO 6-15 zero-ohm resistors can be removed if GPIO function is needed and the secondary functions interfere with GPIO operation. Memory address pins 12-20 are used for Flash only; it is assumed that the Flash and XScale will not be used concurrently, so these zero-ohm resistors may remain populated.

5 Board Drawings and Component Locations

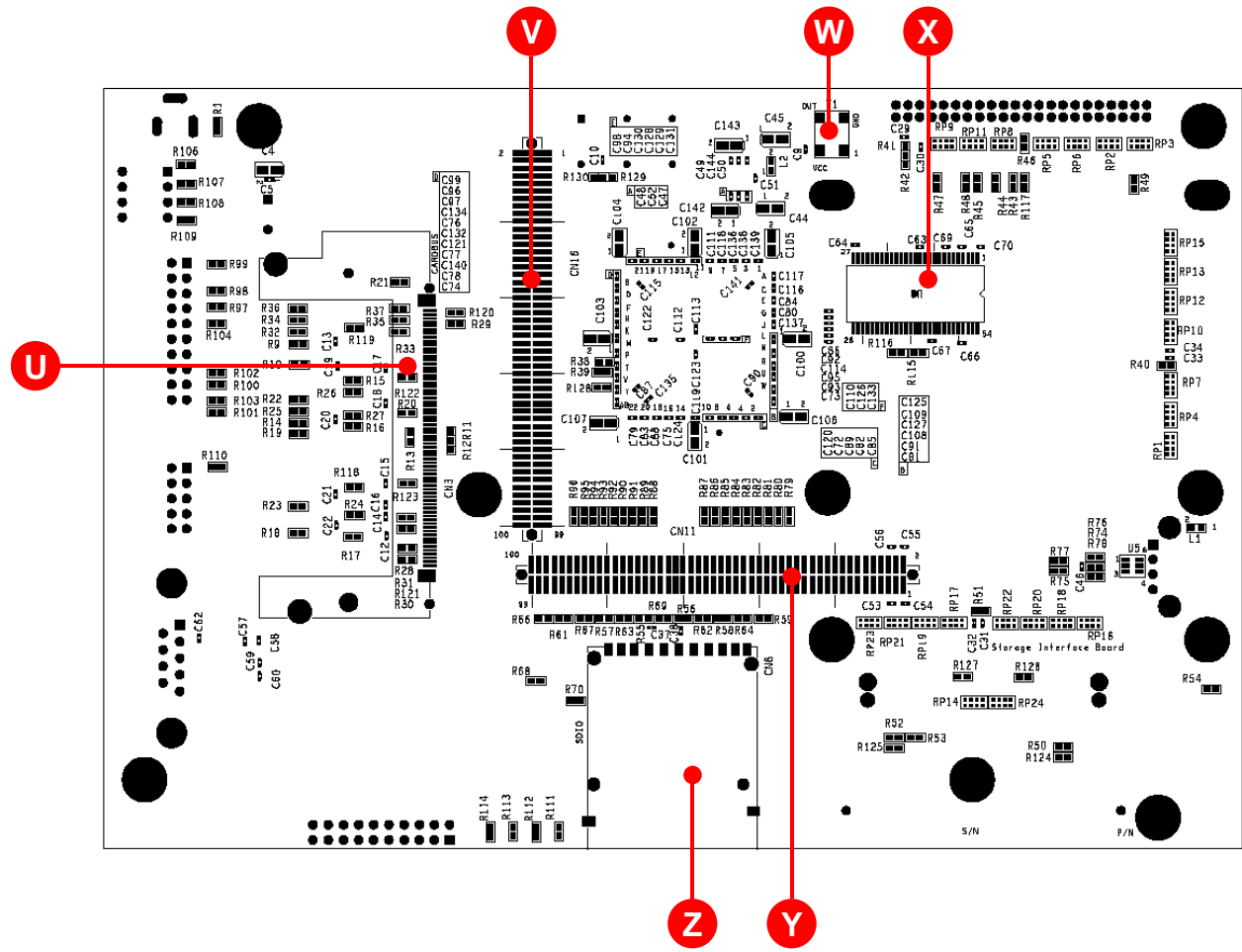
5.1.1 Top Side



item	Description
A	User button
B	Reset button
C	USB 2.0 Host connector
D	FPC IDE connector
E	2.5" HDD IDE connector
F	2M x 16-bit NOR Flash
G	A3PE600-FG484 FPGA
H	User oscillator socket
I	2 A fuse
J	5V power jack

Item	Description
K	3 user DIP switches
L	CoreM7 JTAG header
M	Mini-PCI host connector
N	FPGA Programming header
O	DB9 RS-232
P	16-bit GPIO header
Q	CE-ATA FPC connector
R	4 user LEDs
S	SDIO receptacle
T	Compact Flash receptacle

5.1.2 Bottom Side



item	Description
U	Cardbus receptacle
V	Secondary motherboard connector
W	33 MHz oscillator

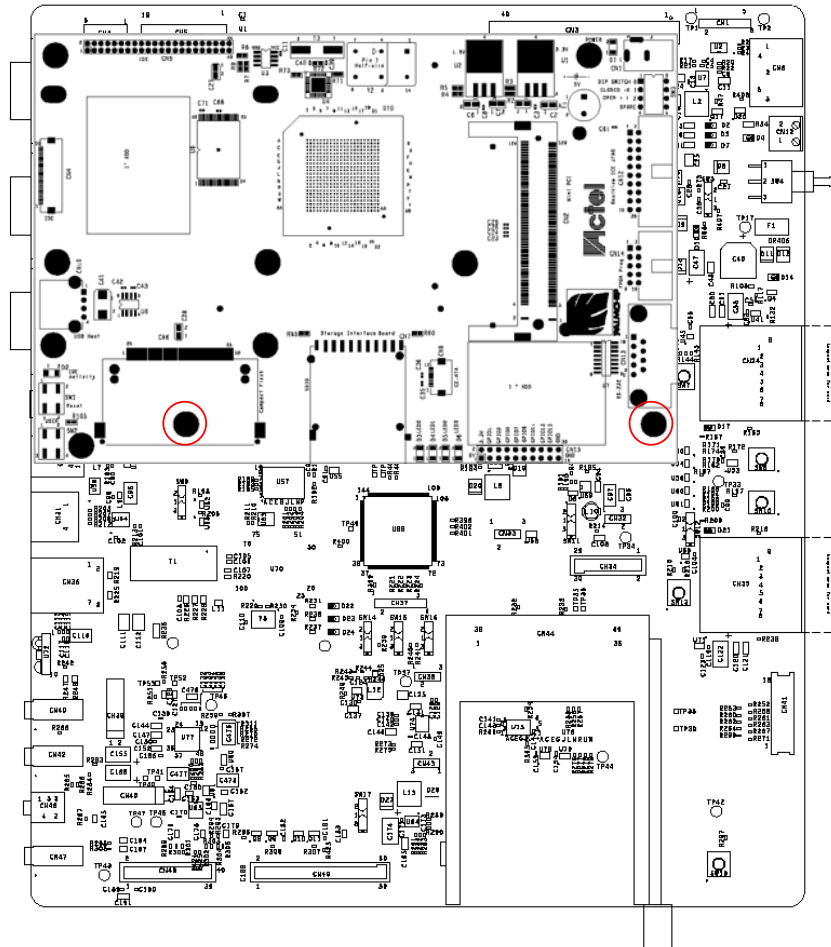
item	Description
X	2M x 16-bit SDRAM
Y	Motherboard connector
Z	SDIO receptacle

6 Board Mounting

6.1 Mounting on BSquare DevKit IDP270 Motherboard

The board can be mounted directly on the motherboard using three or four standoffs. Two of the standoffs mount to the motherboard; the other standoffs provide mechanical support.

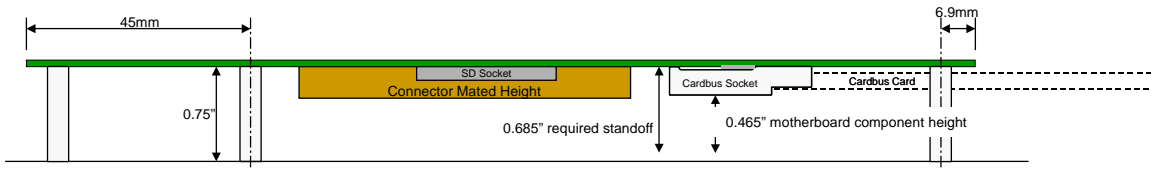
6.1.1 Top View



The standoffs to be screwed through the mounting holes on the motherboard are indicated in red above.

6.1.2 Front View

(Only components on bottom are shown.)



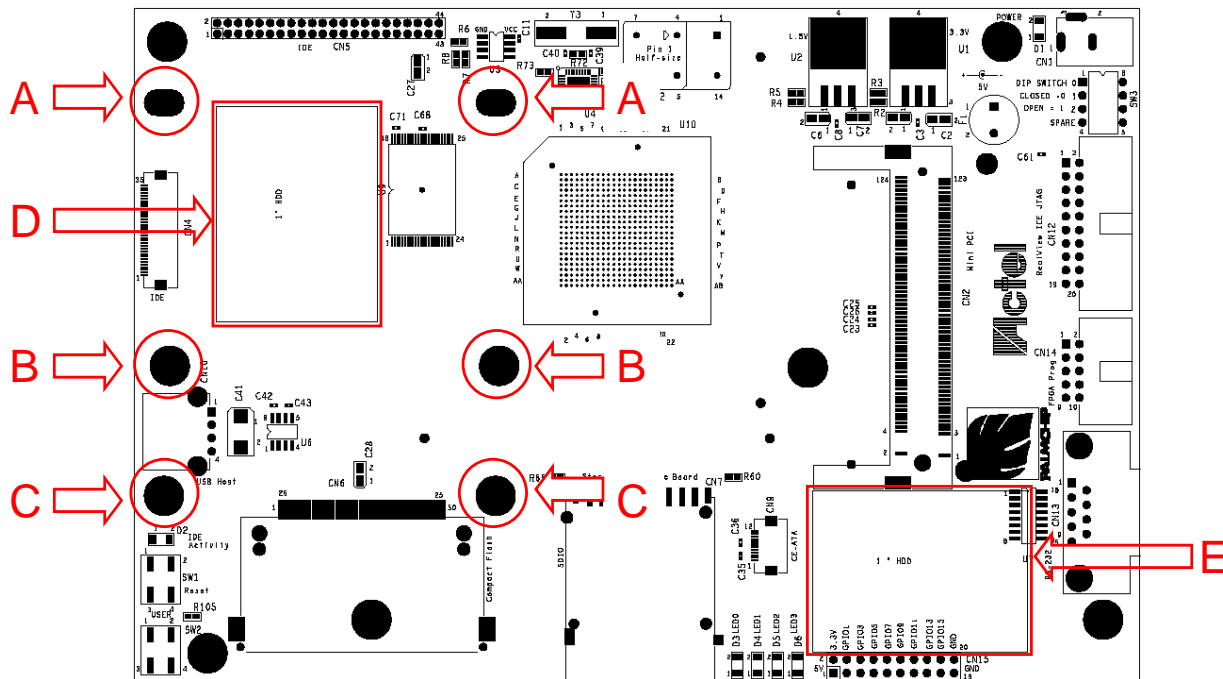
The board should be supported with 3/4-inch (or higher) standoffs due to component height on the motherboard. Plastic standoffs are recommended. The rear standoffs may need to be shaved to accommodate component height under the mounting holes. Because the mating connectors are short relative to the component heights, a flex cable is recommended to connect the daughterboard to the motherboard. See Section 9, “Recommended Parts” for the parts list.

6.1.3 Support for Different Motherboards

A different motherboard may be used. However, if the mating connector does not match, a custom adapter (PCB or flex) may be required. If more signals are required than the 59 available on the primary motherboard connector (CN11), the secondary connector (CN16) may also be used at the expense of the Mini-PCI/Cardbus interfaces.

6.2 Mounting Components on Daughterboard

Refer to the figure below for component mounting locations.



6.2.1 1.8” IDE HDD

Mount the hard drive on standoffs using holes marked “A” and “B”. Some misalignment may occur.

6.2.2 2.5" IDE HDD

Mount the hard drive on standoffs using holes marked "A" and "C". Some misalignment may occur.

6.2.3 1.0" IDE HDD

Mount the hard drive in the area marked "D". Because these drives do not include screw holes for mounting, double-sided tape, hook-and-loop fastener or some similar fastener may be used.

6.2.4 1.0" CE-ATA HDD

Mount the hard drive in the area marked "E". Because these drives do not include screw holes for mounting, double-sided tape, hook-and-loop fastener or some similar fastener may be used.

6.2.5 Compact Flash

Slide the card into the Compact Flash receptacle. To remove, hold the board firmly and pull the card from the receptacle.

6.2.6 SDIO

The MMC/SD/SDIO receptacles included push-push ejectors. To insert, push the card into the receptacle as far as it will go and release it. To remove, push the card in the receptacle as far as it will go, and release; pull the card from the receptacle.

6.2.7 Mini-PCI

Holding the Mini-PCI card at a 45 degree angle, push the card contacts into the socket as far as the card will go, then rotate the free end of the card down until it is parallel to the board; it should be held in place by the tabs on the socket. To remove the card, pull both tabs outward;; the Mini-PCI card should rotate up slightly; release the tabs; the card should remain free from the tabs; pull the card out, away from the connector.

6.2.8 CardBus

Align the card face down with the receptacle. Push the card into the receptacle as far as it will go. To remove the card, hold the board firmly and pull the card from the receptacle.

6.2.9 USB

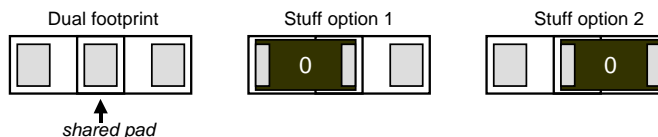
Insert the cable or device into the socket. To remove, pull the cable or device from the socket.

7 Dual Footprints

To prevent power shorts, all power selection jumpers are implemented as dual footprints, with the center pad common to both configurations. The auxiliary oscillator socket is also a dual footprint, allowing the use of a full-size or half-size oscillator socket.

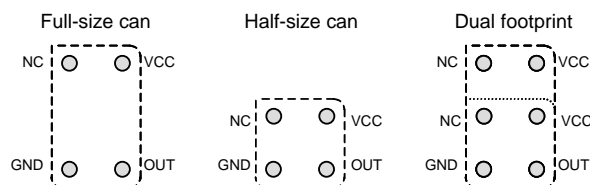
7.1 Resistor Jumpers

Resistor Jumpers share the common pad to prevent both options from being concurrently selected, as illustrated below.



7.2 Can Oscillator

The can oscillator symbol is an overlay of a full-size and a half-size oscillator to allow the use of either oscillator package. The footprints share the ground and output pins, as illustrated below.



8 Connector Pinout

Non-standard connector pinouts are given here. See the relevant standard definitions for the pinouts of all other interfaces.

8.1 Power Jack (CN1)

Pin	Name	Function
Center pin	-	Ground
Barrel	+	+5V

8.2 CE-ATA (CN9)

Pin	Name	Function
1	GND	Ground
2	DAT2	Data bit 2
3	DAT3	Data bit 3
4	VCC	Power
5	CMD	Command
6	VCC	Power
7	CLK	Clock
8	GND	Ground
9	DAT0	Data bit 0
10	DAT1	Data bit 1
11	GND	Ground
12		Reserved

8.3 Motherboard Connectors (CN11 and CN16)

Pin	Name	Function
1	3.3V	(Unused)
3	3.3V	(Unused)
5	GND	Ground
7	A0	(Unused)

Pin	Name	Function
2	5V	5V input
4	5V	5V input
6	GND	Ground
8	NC	(Unused)

9	A1	(Unused)	10	D0	VLIO Data bit 0
11	A2	VLIO Address bit 2	12	D1	VLIO Data bit 1
13	A3	VLIO Address bit 3	14	D2	VLIO Data bit 2
15	A4	VLIO Address bit 4	16	D3	VLIO Data bit 3
17	A5	VLIO Address bit 5	18	D4	VLIO Data bit 4
19	A6	VLIO Address bit 6	20	D5	VLIO Data bit 5
21	A7	VLIO Address bit 7	22	D6	VLIO Data bit 6
23	A8	VLIO Address bit 8	24	D7	VLIO Data bit 7
25	A9	VLIO Address bit 9	26	D8	VLIO Data bit 8
27	A10	VLIO Address bit 10	28	D9	VLIO Data bit 9
29	A11	VLIO Address bit 11	30	D10	VLIO Data bit 10
31	A12	VLIO Address bit 12	32	D11	VLIO Data bit 11
33	A13	VLIO Address bit 13	34	D12	VLIO Data bit 12
35	A14	VLIO Address bit 14	36	D13	VLIO Data bit 13
37	A15	VLIO Address bit 15	38	D14	VLIO Data bit 14
39	A16	VLIO Address bit 16	40	D15	VLIO Data bit 15
41	A17	VLIO Address bit 17	42	D16	VLIO Data bit 16
43	A18	VLIO Address bit 18	44	D17	VLIO Data bit 17
45	A19	(Unused)	46	D18	VLIO Data bit 18
47	A20	(Unused)	48	D19	VLIO Data bit 19
49	A21	(Unused)	50	D20	VLIO Data bit 20
51	A22	(Unused)	52	D21	VLIO Data bit 21
53	A23	(Unused)	54	D22	VLIO Data bit 22
55	A24	(Unused)	56	D23	VLIO Data bit 23
57	A25	(Unused)	58	D24	VLIO Data bit 24
59	NC	(Unused)	60	D25	VLIO Data bit 25
61	DQM0		62	D26	VLIO Data bit 26
63	DQM1		64	D27	VLIO Data bit 27
65	DQM2		66	D28	VLIO Data bit 28
67	DQM3		68	D29	VLIO Data bit 29
69	nCS4	VLIO chip select 4	70	D30	VLIO Data bit 30
71	nCS5	VLIO chip select 5	72	D31	VLIO Data bit 31
73	EXPnCS	VLIO sub-chip select 3	74	nCS1	VLIO chip select 1
75	NC	(Unused)	76	NC	(Unused)
77	RDnWR	(Unused)	78	DVAL0	Companion chip data valid
79	nOE	VLIO output enable	80	DREQ0	Companion chip data request
81	nWE	Memory write enable	82	NC	(Unused)
83	nPWE	VLIO write enable	84	RDY	VLIO ready
85	PWREN	Power enable	86	NC	(Unused)
87	NC	(Unused)	88	NC	(Unused)
89	PERnRESET	Peripheral reset	90	IRQ	Interrupt
91	nRESETOUT	Raw reset	92	NC	(Unused)
93	NC	(Unused)	94	NC	(Unused)
95	GND	Ground	96	GND	Ground
97	GND	Ground	98	GND	Ground
99	GND	Ground	100	GND	Ground

8.4 JTAG ICE (CN12)

Pin	Name	Function
1	VTREF	3.3V
3	TRST	JTAG Reset
5	TDI	JTAG data in
7	TMS	JTAG test mode select

Pin	Name	Function
2	VSUPPLY	3.3V
4	GND	Ground
6	GND	Ground
8	GND	Ground

9	TCK	JTAG clock	10	GND	Ground
11	RTCK	JTAG return clock	12	GND	Ground
13	TDO	JTAG data out	14	GND	Ground
15	SRST	Debugger reset	16	GND	Ground
17	DBGREQ	Debugger request	18	GND	Ground
19	DBGACK	Debugger acknowledge	20	GND	Ground

8.5 RS-232 (CN13)

Pin	Name	Function
1	DCD	DTR loopback
2	TXD	Transmit data
3	RXD	Receive data
4	DTR	Flow control signal
5	GND	Ground
6	DSR	DTR loopback
7	RTS	Flow control signal
8	CTS	RTS loopback
9	RI	(Unused)

8.6 Programming Header (CN14)

Pin	Name	Function	Pin	Name	Function
1	TCK	JTAG clock	2	GND	Ground
3	TDO	JTAG data out	4		(Unused)
5	TMS	JTAG test mode select	6	VJTAG	3.3V
7	VPUMP	3.3V	8	TRST	JTAG reset
9	TDI	JTAG data in	10	GND	Ground

8.7 GPIO Header (CN15)

Pin	Name	Function	Pin	Name	Function
1	5V	5V (after the fuse)	2	3.3V	3.3V
3	GPIO0	GPIO bit 0	4	GPIO1	GPIO bit 1
5	GPIO2	GPIO bit 2	6	GPIO3	GPIO bit 3
7	GPIO4	GPIO bit 4	8	GPIO5	GPIO bit 5
9	GPIO6	GPIO bit 6	10	GPIO7	GPIO bit 7
11	GPIO8	GPIO bit 8	12	GPIO9	GPIO bit 9
13	GPIO10	GPIO bit 10	14	GPIO11	GPIO bit 11
15	GPIO12	GPIO bit 12	16	GPIO13	GPIO bit 13
17	GPIO14	GPIO bit 14	18	GPIO15	GPIO bit 15
19	GND	Ground	20	GND	Ground

8.8 Fuse (F1)

The fuse is not polarized.

8.9 DIP Switch (SW3)

Pin	Name	Function
1		DIP Switch bit 0
2		DIP Switch bit 1
3		DIP Switch bit 2
4		(Unused)


9 Recommended Parts

Recommended parts (or equivalent crosses) that might be needed to connect the demo board to a motherboard are listed below.

Part	Description	Manufacturer	Manufacturer Part Number
CN11	Motherboard Connector	Samtec	SFM-150-02-S-D
CN16	Motherboard Connector	Samtec	SFM-150-02-S-D
F1	Fuse	Wickmann	56000001319
	Flex cable	Samtec	TFMDL-50-T-05.00

10 BSQUARE Board Datasheet


DATASHEET



Trusted Solutions for Smart Devices

DevkitIDP 270 Development Platform

Accelerate time to market for building custom embedded devices



DevkitIDP 270 Layout Offers Quick Access to Hardware

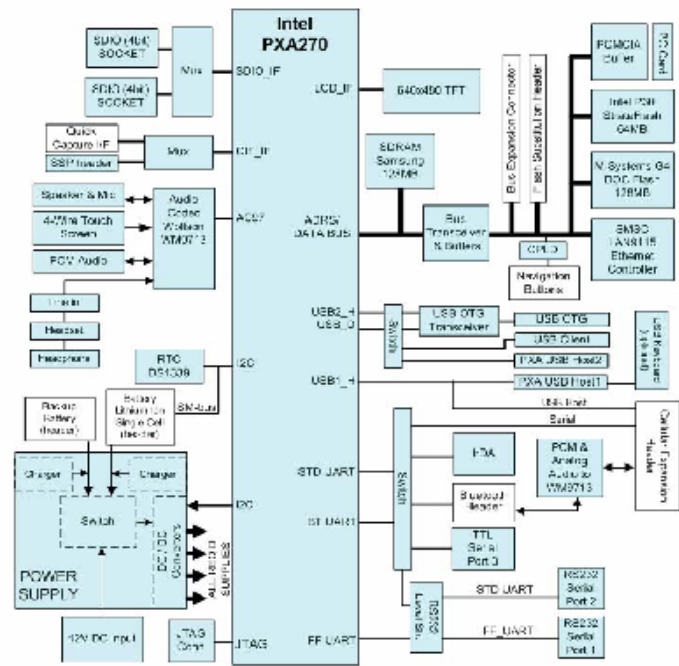
Highlights

- Intel® PXA270 and Windows® CE 5.0
- Quick hardware prototyping and validation
 - o Peripheral expansion bus
 - Test a new display or USB controller
 - o Cellular expansion headers
 - GSM/GPRS, CDMA
 - o SDIO Slot expansion
 - WLAN 802.11 b/g
- Enables parallel software development
 - o Includes Windows CE 5.0 binary BSP
 - o Production-quality software
- Layout enables easy access to hardware
 - o Quick access to test points
 - o Shorter debug time
- RoHS compliant

Overview

The DevkitIDP 270 is a hardware development platform running Windows CE 5.0 that accelerates time to market for OEMs developing custom embedded devices using the Intel® PXA270 Processor. The product includes:

- Intel PXA270 Hardware Platform
- Binary Windows CE 5.0 BSP (nk.bin)
- Documentation
 - o Hardware Reference
 - o Quickstart Guide
 - o Software Guide
 - o Test Documentation
 - o Schematics (pdf)
 - o Bill of Materials (pdf)



DevkitIDP 270 Block Diagram

DATASHEET (P.2)

Hardware Development Platform



Trusted Solutions for Smart Devices

Quickly Prototype Hardware

Hardware engineers can quickly prototype and validate new, custom designs using the peripheral expansion bus, multiple expansion headers including support for GSM/GPRS or CDMA radio and WLAN 802.11 b/g radio, high-resolution display, and different connectivity and storage options on the platform.

Develop Software in Parallel

Software engineers can develop application and system level software in parallel in a target environment close to their end product. This approach eliminates the time needed to migrate code to final hardware. OEMs save time because the product includes a binary production-quality Windows CE 5.0 board support package.

Lower BSP Development Costs

The DevkitIDP 270 is the only Intel PXA270 hardware development platform available with its own tool chain for updating and maintaining its Windows CE board support package (BSP): SchemaBSP. If the DevkitIDP 270 design is used as the basis for the final hardware, SchemaBSP automates updating and maintenance of the binary DevkitIDP 270 BSP as hardware engineers revise the design. SchemaBSP reduces BSP development cost by up to 50 %.

Additional products and services available for the DevkitIDP 270

- SchemaBSP Software Tool
- BSP JumpStart Kit
- DevkitIDP 270 Hardware Design Kit
- Engineering Support and Services
- Windows CE 5.0 Training

Hardware Development Platform Specs	
Processor	Intel XScale PXA 270 RISC microprocessor
Operating System	Windows CE 5.0 production ready BSP
Memory	128MB SDRAM onboard
	64MB Intel StrataFlash (NOR)
	128MB M-Systems NAND Flash
Display	10.4" VGA TFT LCD
	LED Backlight, Dimming control
Input	4-wire resistive touch screen
	Keypad 5-way navigation
Audio	AC'97 Audio and Touch Codec (Wolfson WM9713)
	PCM audio support to cellular header
Ethernet	10/100 Base-T Ethernet controller (SMSC 9115)
USB	1 x Full-speed client or OTG
	2 x Full-speed host
Serial	Full function RS232 port
	Standard RS232 port
	IrDA SIR/FIR
	Bluetooth UART TTL level port
Memory Card Expansion	Two 4-bit SDIO slots
	PCMCIA Type II interface
Expansion slots	Cellular Expansion header (GSM and CDMA)
	Peripheral Expansion bus
	FLASH substitution header
	Video/Camera interface header
	SSP connector with power
	I2C connector
	Power substitution header for PMIC
Power	3.6V Lithium-Ion Primary Battery header
	Speedstep supported core voltage
	Smart Battery SM-Bus I/F
	Battery removal logic
Debug	JTAG interface
Keyboard	USB keyboard
System level Software & Documentation	
Windows CE 5.0	Production ready binary BSP (Bootloader, OAL & device drivers) CE 5.0 binary OS Image (nk.bin)
Hardware Technical Reference	DevKit IDP block diagram, parts placement etc.
Other documentation	QuickStart Guide, Software Guide, Test documentation
HW Schematics	PDF format
Design Source format *	OrCAD Schematic, Allegro layout

* Can be purchased separately

Contact BSQUARE Today

Accelerate time to market for your device: contact BSQUARE today to learn more about the DevkitIDP 270. Call 1-888-820-4500 or 1-425-519-5900 or email sales@bsquare.com

About BSQUARE:

BSQUARE is a solution provider to the global embedded device community. Our teams collaborate with OEMs at any stage in their device development to bring quality products to market faster. Since 1994, BSQUARE has become a trusted partner to smart device makers worldwide.

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