

# Migrating Designs from A3P250 to Lower-Logic-Density Devices

## Introduction

The purpose of this document is to assist you in migrating designs from a high-density ProASIC<sup>®</sup>3 device (A3P250) to lower-density devices (A3P125, A3P060, and A3P030). Since one of the key factors is pin compatibility for a given package among the devices within the family, the primary focus of this document will be to address the pin compatibility issue.

## Design Migration

ProASIC3 family devices are architecturally compatible with each other. However, customers must pay attention to a few key areas when migrating a design. The specific issues discussed throughout this application note are as follows:

- "Design and Device Evaluation"
- "Device and Package Compatibility" on page 2
- "Migration and Implementation Methodologies" on page 2
- "I/O Banks and Standards" on page 3
- "Power Supply Considerations" on page 4
- "Pin Migration and Compatibility" on page 5

## Design and Device Evaluation

When migrating a design, the primary task should be to compare the available resources between two devices. You need to evaluate effective gate count, RAM size, I/O banks, and the number of I/Os. In addition, when porting designs to new ProASIC3 derivatives, timing analysis and simulations should also be validated. Table 1 gives a summary of device resources for the A3P250 device and its smaller migration targets.

**Table 1 • Device Information**

	<b>A3P250</b>	<b>A3P125</b>	<b>A3P060</b>	<b>A3P030</b>
System Gates	250 k	125 k	60 k	30 k
Tiles (D-flip-flops)	6,144	3,072	1,536	768
RAM (kbits)	36	36	18	–
RAM Blocks (4,608 bits)	8	8	4	–
I/O Banks (+ JTAG)	4	2	2	2
User I/Os per Package:				
VQ100	68/13	71	71	77
QN132	87/19	84	80	81
TQ144		100	91	
FG144	97/24	97	96	
PQ208	151/34	133		
FG256	157/38			

*Note: User I/O is given as X (single-ended) or X/Y (single-ended/double-ended).*

## Device and Package Compatibility

ProASIC3 devices and packaging were designed to allow considerable footprint compatibility for smoother migration.

### Common and Convertible I/Os among A3P030, A3P060, A3P125, and A3P250

Table 2 shows the number of I/Os that are common between any two of the above four devices. In addition, the table indicates the number of I/Os that require the necessary conversion (convertible I/Os) using suggested design migration rules in the "Migration and Implementation Methodologies" section.

**Table 2 • Common and Convertible I/Os**

Package	A3P250 A3P125		A3P250 A3P060		A3P250 A3P030		A3P125 A3P060		A3P125 A3P030		A3P060 A3P030	
	Common I/Os	Convertible I/Os	Common I/Os	Convertible I/Os	Common I/Os	Convertible I/Os	Common I/Os	Convertible I/Os	Common I/Os	Convertible I/Os	Common I/Os	Convertible I/Os
VQ100	68	7	67	5	69	46	69	4	72	46	71	46
QN132	84	13	80	25	64	72	80	14	66	70	61	75
FG144	97	–	96	–	N/A	N/A	96	–	N/A	N/A	N/A	N/A
PQ208	134	18	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
TQ144	N/A	N/A	N/A	N/A	N/A	N/A	90	19	N/A	N/A	N/A	N/A

## Migration and Implementation Methodologies

Table 3 on page 3 lists some possible migration combinations and the recommended implementation rules for compatible design conversions from higher-density to lower-density devices. The "Pin Migration and Compatibility" section on page 5 contains tables that list the required rules for different pin combinations. If "Rule x" is mentioned for a pin combination, that combination requires the implementation methodology given in Table 3 on page 3. Note that many combinations of high-density/low-density pins require none of these rules; the pins have complete type compatibility. These pins are marked in the pin tables with "None."

**Table 3 • Migration Rules from Higher-Density Device to Lower-Density Device**

Migration Rule	Issue		Implementation Methodology
	Higher Density	Lower Density	
1	I/O or Global I/O	NC	Leave this pin floating OR program the I/O as unused (software cannot program NC to usable I/O).
	NC	I/O or Global I/O	
2	I/O	Global I/O	Instantiate the global I/O as an I/O buffer (works as a single-ended I/O).
3	Global I/O	I/O	Use the PDC constraint to promote the single-ended I/O to a global pin. There will be some additional delay.
4	VCC or VCCI	NC	The pin can remain connected to the board's VCC, VCCI, VMV, VCOMPLF, or GNDQ plane, as applicable.
	GNDQ	NC	
	VMV	NC	
	VCOMPLF	NC	
5	VCCIB(x) <sup>1</sup>	VCCIB(y) <sup>2</sup>	Make sure the two bank voltage levels are same.
	VMV(x) <sup>1</sup>	VMV(y) <sup>2</sup>	Tie the pin to the board's corresponding VCCI/VMV plane.
6	VMV0	I/O or Global I/O	Leave the pin connected to the board's VCC, VCCI, VMV, VCOMPLF, or GNDQ plane, as applicable. Instantiate the I/O as a tristate buffer with OE = 0 and no weak pull-ups/-downs.
	GNDQ	I/O	
	GNDQ	Global I/O	
	I/O	VCC	
	VCC	I/O	
	VCOMPLF	I/O	
	VCCPLF	I/O	

**Notes:**

1. "x" is a bank number designator and can be 0–3 for ProASIC3 and 0–7 for ProASIC3E.
2. "y" is a bank number designator and can be 0–3 for ProASIC3 and 0–7 for ProASIC3E.

## I/O Banks and Standards

ProASIC3 I/Os are partitioned into multiple I/O voltage banks. The number of banks is device-dependent. There are four I/O banks in the A3P250 device and two I/O banks in the A3P030, A3P060, and A3P125 devices.

Package pins routed to banks 0 and 1 in the A3P250 device are routed to bank 0 in the A3P030, A3P060, and A3P125 devices, and banks 2 and 3 in the A3P250 device are routed to bank 1 in the A3P030, A3P060, and A3P125 devices.

The banks have dedicated supplies; therefore, only I/Os with compatible voltage standards can be assigned to the same I/O voltage bank.

Note that the A3P250 device supports double-ended I/Os; however, the A3P030, A3P060, and A3P125 devices do not support double-ended I/Os.

## Power Supply Considerations

I/O power supply requirements are very important for design migration. Since the migration is within the ProASIC3 family, there is no issue with respect to the core voltage  $V_{CC}$ . Pins that must be appropriately connected are VCCIBx (bank supply voltage to I/O output buffer and I/O logic), VMVx (quiet I/O supply voltage), GNDQ (quiet GND), and GND. GNDQ and VMVx are important to decouple simultaneous switching noise (SSO) for I/Os—enhancing signal integrity and improving noise immunity.

The key rules of migration for the above-mentioned pins are as follows:

- VMV and VCCI values of the higher-density device in a given bank must correspond to the same VMV and VCCI values in the smaller device's migrating bank.
- Since banks 0 and 1 are connected to bank 0 in the smaller device—and banks 2 and 3 are connected to bank 1 in the smaller device—this implies that banks 0 and 1 in the A3P250 device must have identical VMV and identical VCCI. Similarly, the VMV and VCCI voltages in banks 2 and 3 of the A3P250 device must be identical.
- VCCIBx pins in unused banks and VMV pins in unused banks must be connected to GND.
- Unused I/Os should be left alone, since the software automatically configures them as inputs with pull-ups.

Any inappropriate connection during the migration may affect overall dynamic or inrush power consumption and might even result in device malfunction.

Additionally, the I/O naming convention in ProASIC3 devices has significant embedded information (e.g., pin location, bank number, signal type, polarity, and clock conditioning). For a detailed explanation, refer to the "[User I/O Naming Convention](#)" section on page 204. For additional information on power issues, refer to the relevant datasheet.

## Pin Migration and Compatibility

### VQ100 Package

**Table 4 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with VQ100 Packaging**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125	Migration Rule between A3P060 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P250 and A3P030
1	GND	GND	GND	GND	None	None	None	None	None	None
2	IO82RSB1	<b>GAA2/IO51RSB1</b>	<b>GAA2/IO67RSB1</b>	<b>GAA2/IO118UDB3</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
3	IO81RSB1	IO52RSB1	IO68RSB1	IO118VDB3	None	None	None	None	None	None
4	<b>IO80RSB1</b>	<b>GAB2/IO53RSB1</b>	<b>GAB2/IO69RSB1</b>	<b>GAB2/IO117UDB3</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
5	IO79RSB1	IO95RSB1	IO132RSB1	IO117VDB3	None	None	None	None	None	None
6	<b>IO78RSB1</b>	<b>GAC2/IO94RSB1</b>	<b>GAC2/IO131RSB1</b>	<b>GAC2/IO116UDB3</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
7	IO77RSB1	IO93RSB1	IO130RSB1	IO116VDB3	None	None	None	None	None	None
8	<b>IO76RSB1</b>	<b>IO92RSB1</b>	<b>IO129RSB1</b>	<b>IO112PSB3</b>	None	None	None	None	None	None
9	GND	GND	GND	GND	None	None	None	None	None	None
10	IO75RSB1	GFB1/IO87RSB1	GFB1/IO124RSB1	GFB1/IO109PDB3	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
11	IO74RSB1	GFB0/IO86RSB1	GFB0/IO123RSB1	GFB0/IO109NDB3	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
12	<b>GEC0/IO73RSB1</b>	<b>VCOMPLF</b>	<b>VCOMPLF</b>	<b>VCOMPLF</b>	None	None	None	<b>Rule 6</b>	<b>Rule 6</b>	<b>Rule 6</b>
13	<b>GEA0/IO72RSB1</b>	<b>GFA0/IO85RSB1</b>	<b>GFA0/IO122RSB1</b>	<b>GFA0/IO108NPB3</b>	None	None	None	None	None	None
14	<b>GEB0/IO71RSB1</b>	<b>VCCPLF</b>	<b>VCCPLF</b>	<b>VCCPLF</b>	None	None	None	<b>Rule 6</b>	<b>Rule 6</b>	<b>Rule 6</b>
15	IO70RSB1	GFA1/IO84RSB1	GFA1/IO121RSB1	GFA1/IO108PPB3	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
16	IO69RSB1	GFA2/IO83RSB1	GFA2/IO120RSB1	GFA2/IO107PSB3	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
17	VCC	VCC	VCC	VCC	None	None	None	None	None	None
18	<b>VCCIB1</b>	<b>VCCIB1</b>	<b>VCCIB1</b>	<b>VCCIB3</b>	None	None	None	None	None	None
19	IO68RSB1	GEC1/IO77RSB1	GEC0/IO111RSB1	GFC2/IO105PSB3	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
20	IO67RSB1	GEB1/IO75RSB1	GEB1/IO110RSB1	GEC1/IO100PDB3	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 4 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with VQ100 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125	Migration Rule between A3P060 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P250 and A3P030
21	IO66RSB1	GEB0/ IO74RSB1	GEB0/ IO109RSB1	GEC0/ IO100NDB3	None	None	None	Rule 3	Rule 3	Rule 3
22	IO65RSB1	GEA1/ IO73RSB1	GEA1/ IO108RSB1	GEA1/ IO98PDB3	None	None	None	Rule 3	Rule 3	Rule 3
23	IO64RSB1	GEA0/ IO72RSB1	GEA0/ IO107RSB1	GEA0/ IO98NDB3	None	None	None	Rule 3	Rule 3	Rule 3
24	IO63RSB1	VMV1	VMV1	VMV3	None	None	None	Rule 6	Rule 6	Rule 6
25	IO62RSB1	GNDQ	GNDQ	GNDQ	None	None	None	Rule 6	Rule 6	Rule 6
26	IO61RSB1	GEA2/ IO71RSB1	GEA2/ IO106RSB1	GEA2/ IO97RSB2	None	None	None	Rule 3	Rule 3	Rule 3
27	IO60RSB1	GEB2/ IO70RSB1	GEB2/ IO105RSB1	GEB2/ IO96RSB2	None	None	None	Rule 3	Rule 3	Rule 3
28	IO59RSB1	GEC2/ IO69RSB1	GEC2/ IO104RSB1	GEC2/ IO95RSB2	None	None	None	Rule 3	Rule 3	Rule 3
29	IO58RSB1	IO68RSB1	IO102RSB1	IO93RSB2	None	None	None	None	None	None
30	IO57RSB1	IO67RSB1	IO100RSB1	IO92RSB2	None	None	None	None	None	None
31	IO56RSB1	IO66RSB1	IO99RSB1	IO91RSB2	None	None	None	None	None	None
32	IO55RSB1	IO65RSB1	IO97RSB1	IO90RSB2	None	None	None	None	None	None
33	IO54RSB1	IO64RSB1	IO96RSB1	IO88RSB2	None	None	None	None	None	None
34	IO53RSB1	IO63RSB1	IO95RSB1	IO86RSB2	None	None	None	None	None	None
35	IO52RSB1	IO62RSB1	IO94RSB1	IO85RSB2	None	None	None	None	None	None
36	IO51RSB1	IO61RSB1	IO93RSB1	IO84RSB2	None	None	None	None	None	None
37	VCC	V <sub>CC</sub>	VCC	VCC	None	None	None	None	None	None
38	GND	GND	GND	GND	None	None	None	None	None	None
39	VCCIB1	VCCIB1	VCCIB1	VCCIB2	None	None	None	None	None	None
40	IO49RSB1	IO60RSB1	IO87RSB1	IO77RSB2	None	None	None	None	None	None
41	IO47RSB1	IO59RSB1	IO84RSB1	IO74RSB2	None	None	None	None	None	None
42	IO46RSB1	IO58RSB1	IO81RSB1	IO71RSB2	None	None	None	None	None	None
43	IO45RSB1	IO57RSB1	IO75RSB1	GDC2/ IO63RSB2	None	Rule 2	Rule 3	None	None	Rule 3
44	IO44RSB1	GDC2/ IO56RSB1	GDC2/ IO72RSB1	GDB2/ IO62RSB2	None	None	None	Rule 3	Rule 3	Rule 3

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 4 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with VQ100 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125	Migration Rule between A3P060 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P250 and A3P030
45	IO43RSB1	GDB2/ IO55RSB1	GDB2/ IO71RSB1	GDA2/ IO61RSB2	None	None	None	Rule 3	Rule 3	Rule 3
46	IO42RSB1	GDA2/ IO54RSB1	GDA2/ IO70RSB1	GNDQ	None	Rule 6	Rule 6	Rule 3	Rule 3	Rule 6
47	TCK	TCK	TCK	TCK	None	None	None	None	None	None
48	TDI	TDI	TDI	TDI	None	None	None	None	None	None
49	TMS	TMS	TMS	TMS	None	None	None	None	None	None
50	Not Bonded	VMV1	VMV1	VMV2	None	None	None	Rule 4	Rule 4	Rule 4
51	GND	GND	GND	GND	None	None	None	None	None	None
52	VPUMP	VPUMP	VPUMP	VPUMP	None	None	None	None	None	None
53	Not Bonded	NC	NC	NC	None	None	None	None	None	None
54	TDO	TDO	TDO	TDO	None	None	None	None	None	None
55	TRST	TRST	TRST	TRST	None	None	None	None	None	None
56	VJTAG	VJTAG	VJTAG	VJTAG	None	None	None	None	None	None
57	IO41RSB0	GDA1/ IO49RSB0	GDA1/ IO65RSB0	GDA1/ IO60USB1	None	None	None	Rule 3	Rule 3	Rule 3
58	IO40RSB0	GDC0/ IO46RSB0	GDC0/ IO62RSB0	GDC0/ IO58VDB1	None	None	None	Rule 3	Rule 3	Rule 3
59	IO39RSB0	GDC1/ IO45RSB0	GDC1/ IO61RSB0	GDC1/ IO58UDB1	None	None	None	Rule 3	Rule 3	Rule 3
60	IO38RSB0	GCC2/ IO43RSB0	GCC2/ IO59RSB0	IO52NDB1	None	Rule 2	Rule 2	Rule 3	Rule 3	None
61	IO37RSB0	GCB2/ IO42RSB0	GCB2/ IO58RSB0	GCB2/ IO52PDB1	None	None	None	Rule 3	Rule 3	Rule 3
62	IO36RSB0	GCA0/ IO40RSB0	GCA0/ IO56RSB0	GCA1/ IO50PDB1	None	None	None	Rule 3	Rule 3	Rule 3
63	GDB0/IO34RSB0	GCA1/ IO39RSB0	GCA1/ IO55RSB0	GCA0/ IO50NDB1	None	None	None	None	None	None
64	GDA0/IO33RSB0	GCC0/ IO36RSB0	GCC0/ IO52RSB0	GCC0/ IO48NDB1	None	None	None	None	None	None
65	GDC0/IO32RSB0	GCC1/ IO35RSB0	GCC1/ IO51RSB0	GCC1/ IO48PDB1	None	None	None	None	None	None
66	VCCIB0	VCCIB0	VCCIB0	VCCIB1	None	None	None	None	None	None

**Notes:**

1. See Table 3 on page 3 for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 4 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with VQ100 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125	Migration Rule between A3P060 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P250 and A3P030
67	GND	GND	GND	GND	None	None	None	None	None	None
68	VCC	VCC	VCC	VCC	None	None	None	None	None	None
69	IO31RSB0	IO31RSB0	IO47RSB0	IO43NDB1	None	None	None	None	None	None
70	<b>IO30RSB0</b>	<b>GBC2/IO29RSB0</b>	<b>GBC2/IO45RSB0</b>	<b>GBC2/IO43PDB1</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
71	<b>IO29RSB0</b>	<b>GBB2/IO27RSB0</b>	<b>GBB2/IO43RSB0</b>	<b>GBB2/IO42PSB1</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
72	IO28RSB0	IO26RSB0	IO42RSB0	IO41NDB1	None	None	None	None	None	None
73	<b>IO27RSB0</b>	<b>GBA2/IO25RSB0</b>	<b>GBA2/IO41RSB0</b>	<b>GBA2/IO41PDB1</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
74	<b>IO26RSB0</b>	<b>VMV0</b>	<b>VMV0</b>	<b>VMV1</b>	None	None	None	<b>Rule 6</b>	<b>Rule 6</b>	<b>Rule 6</b>
75	<b>IO25RSB0</b>	<b>GNDQ</b>	<b>GNDQ</b>	<b>GNDQ</b>	None	None	None	<b>Rule 6</b>	<b>Rule 6</b>	<b>Rule 6</b>
76	<b>IO24RSB0</b>	<b>GBA1/IO24RSB0</b>	<b>GBA1/IO40RSB0</b>	<b>GBA1/IO40RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
77	<b>IO23RSB0</b>	<b>GBA0/IO23RSB0</b>	<b>GBA0/IO39RSB0</b>	<b>GBA0/IO39RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
78	<b>IO22RSB0</b>	<b>GBB1/IO22RSB0</b>	<b>GBB1/IO38RSB0</b>	<b>GBB1/IO38RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
79	<b>IO21RSB0</b>	<b>GBB0/IO21RSB0</b>	<b>GBB0/IO37RSB0</b>	<b>GBB0/IO37RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
80	<b>IO20RSB0</b>	<b>GBC1/IO20RSB0</b>	<b>GBC1/IO36RSB0</b>	<b>GBC1/IO36RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
81	<b>IO19RSB0</b>	<b>GBC0/IO19RSB0</b>	<b>GBC0/IO35RSB0</b>	<b>GBC0/IO35RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
82	IO18RSB0	IO18RSB0	IO32RSB0	IO29RSB0	None	None	None	None	None	None
83	IO17RSB0	IO17RSB0	IO28RSB0	IO27RSB0	None	None	None	None	None	None
84	IO16RSB0	IO15RSB0	IO25RSB0	IO25RSB0	None	None	None	None	None	None
85	IO15RSB0	IO13RSB0	IO22RSB0	IO23RSB0	None	None	None	None	None	None
86	IO14RSB0	IO11RSB0	IO19RSB0	IO21RSB0	None	None	None	None	None	None
87	VCCIB0	VCCIB0	VCCIB0	VCCIB0	None	None	None	None	None	None
88	GND	GND	GND	GND	None	None	None	None	None	None
89	VCC	VCC	VCC	VCC	None	None	None	None	None	None
90	IO12RSB0	IO10RSB0	IO15RSB0	IO15RSB0	None	None	None	None	None	None
91	IO10RSB0	IO09RSB0	IO13RSB0	IO13RSB0	None	None	None	None	None	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 4 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with VQ100 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125	Migration Rule between A3P060 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P250 and A3P030
92	IO08RSB0	IO08RSB0	IO11RSB0	IO11RSB0	None	None	None	None	None	None
93	IO07RSB0	GAC1/ IO07RSB0	IO09RSB0	GAC1/ IO05RSB0	Rule 2	None	Rule 3	Rule 3	None	Rule 3
94	IO06RSB0	GAC0/ IO06RSB0	IO07RSB0	GAC0/ IO04RSB0	Rule 2	None	Rule 3	Rule 3	None	Rule 3
95	IO05RSB0	GAB1/ IO05RSB0	GAC1/ IO05RSB0	GAB1/ IO03RSB0	None	None	None	Rule 3	Rule 3	Rule 3
96	IO04RSB0	GAB0/ IO04RSB0	GAC0/ IO04RSB0	GAB0/ IO02RSB0	None	None	None	Rule 3	Rule 3	Rule 3
97	IO03RSB0	GAA1/ IO03RSB0	GAB1/ IO03RSB0	GAA1/ IO01RSB0	None	None	None	Rule 3	Rule 3	Rule 3
98	IO02RSB0	GAA0/ IO02RSB0	GAB0/ IO02RSB0	GAA0/ IO00RSB0	None	None	None	Rule 3	Rule 3	Rule 3
99	IO01RSB0	IO01RSB0	GAA1/ IO01RSB0	GNDQ	Rule 3	Rule 6	Rule 6	None	Rule 3	Rule 6
100	IO00RSB0	IO00RSB0	GAA0/ IO00RSB0	VMV0	Rule 3	Rule 6	Rule 6	None	Rule 3	Rule 6

*Notes:*

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

## QFN132 Package

**Table 5 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with QFN132 Packaging**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P060 and A3P030
A1	IO01RSB1	GAB2/ IO00RSB1	GAB2/ IO69RSB1	GAB2/ IO117UPB3	None	None	None	Rule 3	Rule 3	Rule 3
A2	IO81RSB1	IO93RSB1	IO130RSB1	IO117VPB3	None	None	None	None	None	None
A3	NC	VCCIB1	VCCIB1	VCCIB3	Rule 5	None	Rule 5	Rule 4	Rule 4	Rule 4
A4	IO80RSB1	GFC1/ IO89RSB1	GFC1/ IO126RSB1	GFC1/ IO110PDB3	None	None	None	Rule 3	Rule 3	Rule 3
A5	GEC0/ IO77RSB1	GFB0/ IO86RSB1	GFB0/ IO123RSB1	GFB0/ IO109NPB3	None	None	None	None	None	None
A6	NC	VCCPLF	VCCPLF	VCCPLF	None	None	None	Rule 4	Rule 4	Rule 4
A7	GEB0/ IO75RSB1	GFA1/ IO84RSB1	GFA1/ IO121RSB1	GFA1/ IO108PPB3	None	None	None	None	None	None
A8	IO73RSB1	GFC2/ IO81RSB1	GFC2/ IO118RSB1	GFC2/ IO105PPB3	None	None	None	Rule 3	Rule 3	Rule 3
A9	NC	IO78RSB1	IO115RSB1	IO103NDB3	None	None	None	Rule 1	Rule 1	Rule 1
A10	VCC	VCC	VCC	VCC	None	None	None	None	None	None
A11	IO71RSB1	GEB1/ IO75RSB1	GEB1/ IO110RSB1	GEA1/ IO98PPB3	None	None	None	Rule 3	Rule 3	Rule 3
A12	IO68RSB1	GEO0/ IO72RSB1	GEO0/ IO107RSB1	GEO0/ IO98NPB3	None	None	None	Rule 3	Rule 3	Rule 3
A13	IO63RSB1	GEC2/ IO69RSB1	GEC2/ IO104RSB1	GEC2/ IO95RSB2	None	None	None	Rule 3	Rule 3	Rule 3
A14	IO60RSB1	IO65RSB1	IO100RSB1	IO91RSB2	None	None	None	None	None	None
A15	NC	VCC	VCC	VCC	None	None	None	None	None	None
A16	IO59RSB1	IO64RSB1	IO99RSB1	IO90RSB2	None	None	None	None	None	None
A17	IO57RSB1	IO63RSB1	IO96RSB1	IO87RSB2	None	None	None	None	None	None
A18	VCC	IO62RSB1	IO94RSB1	IO85RSB2	None	None	None	Rule 6	Rule 6	Rule 6
A19	IO54RSB1	IO61RSB1	IO91RSB1	IO82RSB2	None	None	None	None	None	None
A20	IO52RSB1	IO58RSB1	IO85RSB1	IO76RSB2	None	None	None	None	None	None
A21	IO49RSB1	GDB2/ IO55RSB1	IO79RSB1	IO70RSB2	None	Rule 2	Rule 2	None	None	Rule 3
A22	IO48RSB1	NC	VCC	VCC	None	Rule 4	Rule 4	Rule 6	Rule 6	Rule 1

**Notes:**

1. See Table 3 on page 3 for the high-density/low-density pin combination guidelines.
2. D pins are corner pins per the package specification.
3. "None" implies that the pins can be connected without any change.

**Table 5 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with QFN132 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P060 and A3P030
A23	IO47RSB1	GDA2/ IO54RSB1	GDB2/ IO71RSB1	GDB2/ IO62RSB2	None	None	None	Rule 3	Rule 3	Rule 3
A24	TDI	TDI	TDI	TDI	None	None	None	None	None	None
A25	TRST	TRST	TRST	TRST	None	None	None	None	None	None
A26	IO44RSB0	GDC1/ IO48RSB0	GDC1/ IO61RSB0	GDC1/ IO58UDB1	None	None	None	Rule 3	Rule 3	Rule 3
A27	NC	VCC	VCC	VCC	None	None	None	Rule 4	Rule 4	Rule 4
A28	IO43RSB0	IO47RSB0	IO60RSB0	IO54NDB1	None	None	None	None	None	None
A29	IO42RSB0	GCC2/ IO46RSB0	GCC2/ IO59RSB0	IO52NDB1	None	None	Rule 2	None	Rule 3	Rule 3
A30	IO40RSB0	GCA2/ IO44RSB0	GCA2/ IO57RSB0	GCA2/ IO51PPB1	None	None	None	Rule 3	Rule 3	Rule 3
A31	IO39RSB0	GCA0/ IO43RSB0	GCA0/ IO56RSB0	GCA0/ IO50NPB1	None	None	None	Rule 3	Rule 3	Rule 3
A32	GDC0/ IO36RSB0	GCB1/ IO40RSB0	GCB1/ IO53RSB0	GCB1/ IO49PDB1	None	None	None	None	None	None
A33	NC	IO36RSB0	IO49RSB0	IO47NSB1	None	None	None	Rule 1	Rule 1	Rule 1
A34	VCC	VCC	VCC	VCC	None	None	None	None	None	None
A35	IO34RSB0	IO31RSB0	IO44RSB0	IO41NPB1	None	None	None	None	None	None
A36	IO31RSB0	GBA2/ IO28RSB0	GBA2/ IO41RSB0	GBA2/ IO41PPB1	None	None	None	Rule 3	Rule 3	Rule 3
A37	IO26RSB0	GBB1/ IO25RSB0	GBB1/ IO38RSB0	GBB1/ IO38RSB0	None	None	None	Rule 3	Rule 3	Rule 3
A38	IO23RSB0	GBC0/ IO22RSB0	GBC0/ IO35RSB0	GBC0/ IO35RSB0	None	None	None	Rule 3	Rule 3	Rule 3
A39	NC	VCCIB0	VCCIB0	VCCIB0	None	None	None	Rule 4	Rule 4	Rule 4
A40	IO22RSB0	IO21RSB0	IO28RSB0	IO28RSB0	None	None	None	None	None	None
A41	IO20RSB0	IO18RSB0	IO22RSB0	IO22RSB0	None	None	None	None	None	None
A42	IO18RSB0	IO15RSB0	IO18RSB0	IO18RSB0	None	None	None	None	None	None
A43	VCC	IO14RSB0	IO14RSB0	IO14RSB0	None	None	None	Rule 6	Rule 6	Rule 6
A44	IO15RSB0	IO11RSB0	IO11RSB0	IO11RSB0	None	None	None	None	None	None
A45	IO12RSB0	GAB1/ IO08RSB0	IO07RSB0	IO07RSB0	None	Rule 2	Rule 2	None	None	Rule 3

**Notes:**

1. See Table 3 on page 3 for the high-density/low-density pin combination guidelines.
2. D pins are corner pins per the package specification.
3. "None" implies that the pins can be connected without any change.

**Table 5 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with QFN132 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P060 and A3P030
A46	IO10RSB0	NC	VCC	VCC	None	Rule 4	Rule 4	Rule 6	Rule 6	Rule 1
A47	IO09RSB0	GAB0/ IO07RSB0	GAC1/ IO05RSB0	GAC1/ IO05RSB0	None	None	None	Rule 3	Rule 3	Rule 3
A48	IO06RSB0	IO04RSB0	GAB0/ IO02RSB0	GAB0/ IO02RSB0	None	Rule 3	Rule 3	Rule 3	Rule 3	None
B1	IO02RSB1	IO01RSB1	IO68RSB1	IO118VDB3	None	None	None	None	None	None
B2	IO82RSB1	GAC2/ IO94RSB1	GAC2/ IO131RSB1	GAC2/ IO116UDB3	None	None	None	Rule 3	Rule 3	Rule 3
B3	GND	GND	GND	GND	None	None	None	None	None	None
B4	IO79RSB1	GFC0/ IO88RSB1	GFC0/ IO125RSB1	GFC0/ IO110NDB3	None	None	None	Rule 3	Rule 3	Rule 3
B5	NC	VCOMPLF	VCOMPLF	VCOMPLF	None	None	None	Rule 4	Rule 4	Rule 4
B6	GND	GND	GND	GND	None	None	None	None	None	None
B7	IO74RSB1	GFB2/ IO82RSB1	GFB2/ IO119RSB1	GFB2/ IO106PSB3	None	None	None	Rule 3	Rule 3	Rule 3
B8	NC	IO79RSB1	IO116RSB1	IO103PDB3	None	None	None	Rule 1	Rule 1	Rule 1
B9	GND	GND	GND	GND	None	None	None	None	None	None
B10	IO70RSB1	GEB0/ IO74RSB1	GEB0/ IO109RSB1	GEB0/ IO99NDB3	None	None	None	Rule 3	Rule 3	Rule 3
B11	IO67RSB1	VMV1	VMV1	VMV3	Rule 6	None	Rule 5	Rule 6	Rule 6	Rule 6
B12	IO64RSB1	GEB2/ IO70RSB1	GEB2/ IO105RSB1	GEB2/ IO96RSB2	None	None	None	Rule 3	Rule 3	Rule 3
B13	IO61RSB1	IO67RSB1	IO101RSB1	IO92RSB2	None	None	None	None	None	None
B14	GND	GND	GND	GND	None	None	None	None	None	None
B15	IO58RSB1	NC	IO98RSB1	IO89RSB2	None	Rule 1	Rule 1	None	None	Rule 1
B16	IO56RSB1	NC	IO95RSB1	IO86RSB2	None	Rule 1	Rule 1	None	None	Rule 1
B17	GND	GND	GND	GND	None	None	None	None	None	None
B18	IO53RSB1	IO59RSB1	IO87RSB1	IO78RSB2	None	None	None	None	None	None
B19	IO50RSB1	GDC2/ IO56RSB1	IO81RSB1	IO72RSB2	None	Rule 2	Rule 2	None	None	Rule 3
B20	GND	GND	GND	GND	None	None	None	None	None	None
B21	IO46RSB1	GNDQ	GNDQ	GNDQ	None	None	None	Rule 6	Rule 6	Rule 6

**Notes:**

1. See Table 3 on page 3 for the high-density/low-density pin combination guidelines.
2. D pins are corner pins per the package specification.
3. "None" implies that the pins can be connected without any change.

**Table 5 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with QFN132 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P060 and A3P030
B22	TMS	TMS	TMS	TMS	None	None	None	None	None	None
B23	TDO	TDO	TDO	TDO	None	None	None	None	None	None
<b>B24</b>	IO45RSB0	<b>GDC0/IO49RSB0</b>	<b>GDC0/IO62RSB0</b>	<b>GDC0/IO58VDB1</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
<b>B25</b>	GND	<b>GND</b>	<b>GND</b>	<b>GND</b>	None	None	None	None	None	None
B26	NC	NC	NC	IO54PDB1	Rule 1	None	Rule 1	Rule 1	None	None
<b>B27</b>	IO41RSB0	<b>GCB2/IO45RSB0</b>	<b>GCB2/IO58RSB0</b>	<b>GCB2/IO52PDB1</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
B28	GND	GND	GND	GND	None	None	None	None	None	None
B29	GDA0/IO37RSB0	GCB0/IO41RSB0	GCB0/IO54RSB0	GCB0/IO49NDB1	None	None	None	None	None	None
<b>B30</b>	NC	<b>GCC1/IO38RSB0</b>	<b>GCC1/IO51RSB0</b>	<b>GCC1/IO48PDB1</b>	None	None	None	<b>Rule 1</b>	<b>Rule 1</b>	<b>Rule 1</b>
B31	GND	GND	GND	GND	None	None	None	None	None	None
<b>B32</b>	IO33RSB0	<b>GBB2/IO30RSB0</b>	<b>GBB2/IO43RSB0</b>	<b>GBB2/IO42PDB1</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
<b>B33</b>	IO30RSB0	<b>VMV0</b>	<b>VMV0</b>	<b>VMV1</b>	<b>Rule 5</b>	<b>None</b>	<b>Rule 5</b>	<b>Rule 6</b>	<b>Rule 6</b>	<b>Rule 6</b>
<b>B34</b>	IO27RSB0	<b>GBA0/IO26RSB0</b>	<b>GBA0/IO39RSB0</b>	<b>GBA0/IO39RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
<b>B35</b>	IO24RSB0	<b>GBC1/IO23RSB0</b>	<b>GBC1/IO36RSB0</b>	<b>GBC1/IO36RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
B36	GND	GND	GND	GND	None	None	None	None	None	None
B37	IO21RSB0	IO20RSB0	IO26RSB0	IO26RSB0	None	None	None	None	None	None
B38	IO19RSB0	IO17RSB0	IO21RSB0	IO21RSB0	None	None	None	None	None	None
B39	GND	GND	GND	GND	None	None	None	None	None	None
B40	IO16RSB0	IO12RSB0	IO13RSB0	IO13RSB0	None	None	None	None	None	None
<b>B41</b>	IO13RSB0	<b>GAC0/IO09RSB0</b>	<b>IO08RSB0</b>	<b>IO08RSB0</b>	None	<b>Rule 2</b>	<b>Rule 2</b>	None	None	<b>Rule 3</b>
B42	GND	GND	GND	GND	None	None	None	None	None	None
<b>B43</b>	IO08RSB0	<b>GAA1/IO06RSB0</b>	<b>GAC0/IO04RSB0</b>	<b>GAC0/IO04RSB0</b>	None	None	None	<b>Rule 3</b>	<b>Rule 3</b>	<b>Rule 3</b>
<b>B44</b>	IO05RSB0	<b>GNDQ</b>	<b>GNDQ</b>	<b>GNDQ</b>	None	None	None	<b>Rule 6</b>	<b>Rule 6</b>	<b>Rule 6</b>

**Notes:**

1. See Table 3 on page 3 for the high-density/low-density pin combination guidelines.
2. D pins are corner pins per the package specification.
3. "None" implies that the pins can be connected without any change.

**Table 5 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with QFN132 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P060 and A3P030
C1	IO03RSB1	<b>GAA2/IO02RSB1</b>	<b>GAA2/IO67RSB1</b>	<b>GAA2/IO118UDB3</b>	None	None	None	Rule 3	Rule 3	Rule 3
C2	IO00RSB1	IO95RSB1	IO132RSB1	IO116VDB3	None	None	None	None	None	None
C3	NC	VCC	VCC	VCC	None	None	None	Rule 4	Rule 4	Rule 4
C4	IO78RSB1	GFB1/IO87RSB1	GFB1/IO124RSB1	GFB1/IO109PPB3	None	None	None	Rule 3	Rule 3	Rule 3
C5	GEO/IO76RSB1	<b>GFA0/IO85RSB1</b>	<b>GFA0/IO122RSB1</b>	<b>GFA0/IO108NPB3</b>	None	None	None	None	None	None
C6	NC	<b>GFA2/IO83RSB1</b>	<b>GFA2/IO120RSB1</b>	<b>GFA2/IO107PSB3</b>	None	None	None	Rule 1	Rule 1	Rule 1
C7	NC	<b>IO80RSB1</b>	<b>IO117RSB1</b>	<b>IO105NPB3</b>	None	None	None	Rule 1	Rule 1	Rule 1
C8	VCCIB1	VCCIB1	VCCIB1	VCCIB3	Rule 5	None	Rule 5	Rule 5	Rule 5	Rule 5
C9	IO69RSB1	<b>GEO/IO73RSB1</b>	<b>GEO/IO108RSB1</b>	<b>GEB1/IO99PDB3</b>	None	None	None	Rule 3	Rule 3	Rule 3
C10	IO66RSB1	<b>GNDQ</b>	<b>GNDQ</b>	<b>GNDQ</b>	None	None	None	Rule 6	Rule 6	Rule 6
C11	IO65RSB1	<b>GEO/IO71RSB1</b>	<b>GEO/IO106RSB1</b>	<b>GEO/IO97RSB2</b>	None	None	None	Rule 3	Rule 3	Rule 3
C12	IO62RSB1	IO68RSB1	IO103RSB1	IO94RSB2	None	None	None	None	None	None
C13	NC	VCCIB1	VCCIB1	VCCIB2	Rule 5	None	Rule 5	Rule 4	Rule 4	Rule 4
C14	NC	NC	<b>IO97RSB1</b>	<b>IO88RSB2</b>	None	Rule 1	Rule 1	Rule 1	Rule 1	None
C15	IO55RSB1	NC	<b>IO93RSB1</b>	<b>IO84RSB2</b>	None	Rule 1	Rule 1	None	None	Rule 1
C16	V <sub>CC</sub> B1	<b>IO60RSB1</b>	<b>IO89RSB1</b>	<b>IO80RSB2</b>	None	None	None	Rule 6	Rule 6	Rule 6
C17	IO51RSB1	IO57RSB1	IO83RSB1	IO74RSB2	None	None	None	None	None	None
C18	NC	NC	VCCIB1	VCCIB2	Rule 5	Rule 4	Rule 4	Rule 4	Rule 4	Rule 4
C19	TCK	TCK	TCK	TCK	None	None	None	None	None	None
C20	NC	<b>VMV1</b>	<b>VMV1</b>	<b>VMV2</b>	None	None	None	Rule 4	Rule 4	Rule 4
C21	VPUMP	VPUMP	VPUMP	VPUMP	None	None	None	None	None	None
C22	VJTAG	VJTAG	VJTAG	VJTAG	None	None	None	None	None	None
C23	NC	VCCIB0	VCCIB0	VCCIB1	Rule 5	None	Rule 5	Rule 4	Rule 4	Rule 4
C24	NC	NC	NC	<b>IO53NSB1</b>	Rule 1	None	Rule 1	Rule 1	None	None
C25	NC	NC	NC	<b>IO51NPB1</b>	Rule 1	None	Rule 1	Rule 1	None	None

**Notes:**

1. See Table 3 on page 3 for the high-density/low-density pin combination guidelines.
2. D pins are corner pins per the package specification.
3. "None" implies that the pins can be connected without any change.

**Table 5 • Pin Compatibility and Migration Table for A3P030, A3P060, A3P125, and A3P250 with QFN132 Packaging (continued)**

Pin No.	A3P030 Function	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P030	Migration Rule between A3P125 and A3P030	Migration Rule between A3P060 and A3P030
C26	GDB0/ IO38RSB0	GCA1/ IO42RSB0	GCA1/ IO55RSB0	GCA1/ IO50PPB1	None	None	None	None	None	None
<b>C27</b>	NC	<b>GCC0/ IO39RSB0</b>	<b>GCC0/ IO52RSB0</b>	<b>GCC0/ IO48NDB1</b>	None	None	None	Rule 1	Rule 1	Rule 1
<b>C28</b>	VCCIB0	VCCIB0	VCCIB0	VCCIB1	Rule 5	None	Rule 5	Rule 5	Rule 5	None
C29	IO32RSB0	IO29RSB0	IO42RSB0	IO42NDB1	None	None	None	None	None	None
<b>C30</b>	IO29RSB0	<b>GNDQ</b>	<b>GNDQ</b>	<b>GNDQ</b>	None	None	None	Rule 6	Rule 6	Rule 6
<b>C31</b>	IO28RSB0	<b>GBA1/ IO27RSB0</b>	<b>GBA1/ IO40RSB0</b>	<b>GBA1/ IO40RSB0</b>	None	None	None	Rule 3	Rule 3	Rule 3
<b>C32</b>	IO25RSB0	<b>GBB0/ IO24RSB0</b>	<b>GBB0/ IO37RSB0</b>	<b>GBB0/ IO37RSB0</b>	None	None	None	Rule 3	Rule 3	Rule 3
<b>C33</b>	NC	VCC	VCC	VCC	None	None	None	Rule 4	Rule 4	Rule 4
<b>C34</b>	NC	<b>IO19RSB0</b>	<b>IO24RSB0</b>	<b>IO24RSB0</b>	None	None	None	Rule 3	Rule 3	Rule 3
<b>C35</b>	VCCIB0	<b>IO16RSB0</b>	<b>IO19RSB0</b>	<b>IO19RSB0</b>	None	None	None	Rule 1	Rule 1	Rule 1
C36	IO17RSB0	IO13RSB0	IO16RSB0	IO16RSB0	None	None	None	None	None	None
<b>C37</b>	IO14RSB0	<b>GAC1/ IO10RSB0</b>	<b>IO10RSB0</b>	<b>IO10RSB0</b>	None	Rule 2	Rule 2	None	None	Rule 3
<b>C38</b>	IO11RSB0	NC	VCCIB0	VCCIB0	Rule 5	Rule 4	Rule 4	Rule 6	Rule 6	Rule 1
<b>C39</b>	IO07RSB0	<b>GAA0/ IO05RSB0</b>	<b>GAB1/ IO03RSB0</b>	<b>GAB1/ IO03RSB0</b>	None	None	None	Rule 3	Rule 3	Rule 3
<b>C40</b>	IO04RSB0	<b>VMV0</b>	<b>VMV0</b>	<b>VMV0</b>	None	None	None	Rule 6	Rule 6	Rule 6
D1	GND	GND	GND	GND	None	None	None	None	None	None
D2	GND	GND	GND	GND	None	None	None	None	None	None
D3	GND	GND	GND	GND	None	None	None	None	None	None
D4	GND	GND	GND	GND	None	None	None	None	None	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. D pins are corner pins per the package specification.
3. "None" implies that the pins can be connected without any change.

## TQ144 Package

**Table 6 • Pin Compatibility and Migration Table for ProASIC3 A3P060 and A3P125 with TQ144 Packaging**

Pin Number	A3P060 Function	A3P125 Function	Migration Rule between A3P125 and A3P060
1	GAA2/IO51RSB1	GAA2/IO67RSB1	None
2	IO52RSB1	IO68RSB1	None
3	GAB2/IO53RSB1	GAB2/IO69RSB1	None
4	IO95RSB1	IO132RSB1	None
5	GAC2/IO94RSB1	GAC2/IO131RSB1	None
6	IO93RSB1	IO130RSB1	None
7	IO92RSB1	IO129RSB1	None
8	IO91RSB1	IO128RSB1	None
9	VCC	VCC	None
10	GND	GND	None
11	VCCIB1	VCCIB1	None
12	IO90RSB1	IO127RSB1	None
13	GFC1/IO89RSB1	GFC1/IO126RSB1	None
14	GFC0/IO88RSB1	GFC0/IO125RSB1	None
15	GFB1/IO87RSB1	GFB1/IO124RSB1	None
16	GFB0/IO86RSB1	GFB0/IO123RSB1	None
17	VCOMPLF	VCOMPLF	None
18	GFA0/IO85RSB1	GFA0/IO122RSB1	None
19	VCCPLF	VCCPLF	None
20	GFA1/IO84RSB1	GFA1/IO121RSB1	None
21	GFA2/IO83RSB1	GFA2/IO120RSB1	None
22	GFB2/IO82RSB1	GFB2/IO119RSB1	None
23	GFC2/IO81RSB1	GFC2/IO118RSB1	None
24	IO80RSB1	IO117RSB1	None
25	IO79RSB1	IO116RSB1	None
26	IO78RSB1	IO115RSB1	None
27	GND	GND	None
28	VCCIB1	VCCIB1	None
29	GEC1/IO77RSB1	GEC1/IO112RSB1	None
30	GEC0/IO76RSB1	GEC0/IO111RSB1	None
31	GEB1/IO75RSB1	GEB1/IO110RSB1	None
32	GEB0/IO74RSB1	GEB0/IO109RSB1	None
33	GEA1/IO73RSB1	GEA1/IO108RSB1	None
34	GEA0/IO72RSB1	GEA0/IO107RSB1	None
35	VMV1	VMV1	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 6 • Pin Compatibility and Migration Table for ProASIC3 A3P060 and A3P125 with TQ144 Packaging (continued)**

Pin Number	A3P060 Function	A3P125 Function	Migration Rule between A3P125 and A3P060
36	GNDQ	GNDQ	None
37	NC	NC	None
38	GEA2/IO71RSB1	GEA2/IO106RSB1	None
39	GEB2/IO70RSB1	GEB2/IO105RSB1	None
40	GEC2/IO69RSB1	GEC2/IO104RSB1	None
41	IO68RSB1	IO103RSB1	None
42	IO67RSB1	IO102RSB1	None
43	IO66RSB1	IO101RSB1	None
44	IO65RSB1	IO100RSB1	None
45	VCC	VCC	None
46	GND	GND	None
47	VCCIB1	VCCIB1	None
48	NC	IO99RSB1	Rule 1
49	IO64RSB1	IO97RSB1	None
50	NC	IO95RSB1	Rule 1
51	IO63RSB1	IO93RSB1	None
52	NC	IO92RSB1	Rule 1
53	IO62RSB1	IO90RSB1	None
54	NC	IO88RSB1	Rule 1
55	IO61RSB1	IO86RSB1	None
56	NC	IO84RSB1	Rule 1
57	NC	IO83RSB1	Rule 1
58	IO60RSB1	IO82RSB1	None
59	IO59RSB1	IO81RSB1	None
60	IO58RSB1	IO80RSB1	None
61	IO57RSB1	IO79RSB1	None
62	NC	VCC	Rule 4
63	GND	GND	None
64	NC	VCCIB1	Rule 4
65	GDC2/IO56RSB1	GDC2/IO72RSB1	None
66	GDB2/IO55RSB1	GDB2/IO71RSB1	None
67	GDA2/IO54RSB1	GDA2/IO70RSB1	None
68	GNDQ	GNDQ	None
69	TCK	TCK	None
70	TDI	TDI	None
71	TMS	TMS	None
72	VMV1	VMV1	None

**Notes:**

1. See Table 3 on page 3 for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 6 • Pin Compatibility and Migration Table for ProASIC3 A3P060 and A3P125 with TQ144 Packaging (continued)**

Pin Number	A3P060 Function	A3P125 Function	Migration Rule between A3P125 and A3P060
73	VPUMP	VPUMP	None
74	NC	NC	None
75	TDO	TDO	None
76	TRST	TRST	None
77	VJTAG	VJTAG	None
78	GDA0/IO50RSB0	GDA0/IO66RSB0	None
79	GDB0/IO48RSB0	GDB0/IO64RSB0	None
80	GDB1/IO47RSB0	GDB1/IO63RSB0	None
81	VCCIB0	VCCIB0	None
82	GND	GND	None
83	IO44RSB0	IO60RSB0	None
84	GCC2/IO43RSB0	GCC2/IO59RSB0	None
85	GCB2/IO42RSB0	GCB2/IO58RSB0	None
86	GCA2/IO41RSB0	GCA2/IO57RSB0	None
87	GCA0/IO40RSB0	GCA0/IO56RSB0	None
88	GCA1/IO39RSB0	GCA1/IO55RSB0	None
89	GCB0/IO38RSB0	GCB0/IO54RSB0	None
90	GCB1/IO37RSB0	GCB1/IO53RSB0	None
91	GCC0/IO36RSB0	GCC0/IO52RSB0	None
92	GCC1/IO35RSB0	GCC1/IO51RSB0	None
93	IO34RSB0	IO50RSB0	None
94	IO33RSB0	IO49RSB0	None
95	NC	NC	None
96	NC	NC	None
97	NC	NC	None
98	VCCIB0	VCCIB0	None
99	GND	GND	None
100	VCC	VCC	None
101	IO30RSB0	IO47RSB0	None
102	GBC2/IO29RSB0	GBC2/IO45RSB0	None
103	IO28RSB0	IO44RSB0	None
104	GBB2/IO27RSB0	GBB2/IO43RSB0	None
105	IO26RSB0	IO42RSB0	None
106	GBA2/IO25RSB0	GBA2/IO41RSB0	None
107	VMV0	VMV0	None
108	GNDQ	GNDQ	None
109	NC	GBA1/IO40RSB0	Rule 1

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 6 • Pin Compatibility and Migration Table for ProASIC3 A3P060 and A3P125 with TQ144 Packaging (continued)**

Pin Number	A3P060 Function	A3P125 Function	Migration Rule between A3P125 and A3P060
110	NC	GBA0/IO39RSB0	Rule 1
111	GBA1/IO24RSB0	GBB1/IO38RSB0	None
112	GBA0/IO23RSB0	GBB0/IO37RSB0	None
113	GBB1/IO22RSB0	GBC1/IO36RSB0	None
114	GBB0/IO21RSB0	GBC0/IO35RSB0	None
115	GBC1/IO20RSB0	IO34RSB0	Rule 2
116	GBC0/IO19RSB0	IO33RSB0	Rule 2
117	VCCIB0	VCCIB0	None
118	GND	GND	None
119	VCC	VCC	None
120	IO18RSB0	IO29RSB0	None
121	IO17RSB0	IO28RSB0	None
122	IO16RSB0	IO27RSB0	None
123	IO15RSB0	IO25RSB0	None
124	IO14RSB0	IO23RSB0	None
125	IO13RSB0	IO21RSB0	None
126	IO12RSB0	IO19RSB0	None
127	IO11RSB0	IO17RSB0	None
128	NC	IO16RSB0	Rule 1
129	IO10RSB0	IO14RSB0	None
130	IO09RSB0	IO12RSB0	None
131	IO08RSB0	IO10RSB0	None
132	GAC1/IO07RSB0	IO08RSB0	Rule 2
133	GAC0/IO06RSB0	IO06RSB0	Rule 2
134	NC	VCCIB0	Rule 4
135	GND	GND	None
136	NC	V <sub>CC</sub>	Rule 4
137	GAB1/IO05RSB0	GAC1/IO05RSB0	None
138	GAB0/IO04RSB0	GAC0/IO04RSB0	None
139	GAA1/IO03RSB0	GAB1/IO03RSB0	None
140	GAA0/IO02RSB0	GAB0/IO02RSB0	None
141	IO01RSB0	GAA1/IO01RSB0	Rule 3
142	IO00RSB0	GAA0/IO00RSB0	Rule 3
143	GNDQ	GNDQ	None
144	VMV0	VMV0	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

## PQ208 Package

**Table 7 • Pin Compatibility and Migration Table for ProASIC3 A3P125 and A3P250 with PQ208 Packaging**

Pin Number	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125
1	GND	GND	None
2	GAA2/IO67RSB1	GAA2/IO118UDB3	None
3	IO68RSB1	IO118VDB3	None
4	GAB2/IO69RSB1	GAB2/IO117UDB3	None
5	IO132RSB1	IO117VDB3	None
6	GAC2/IO131RSB1	GAC2/IO116UDB3	None
7	NC	IO116VDB3	Rule 1
8	NC	IO115UDB3	Rule 1
9	IO130RSB1	IO115VDB3	None
10	IO129RSB1	IO114UDB3	None
11	NC	IO114VDB3	Rule 1
12	IO128RSB1	IO113PDB3	None
13	NC	IO113NDB3	Rule 1
14	NC	IO112PDB3	Rule 1
15	NC	IO112NDB3	Rule 1
16	VCC	VCC	None
17	GND	GND	None
18	VCCIB1	VCCIB3	Rule 5
19	IO127RSB1	IO111PDB3	None
20	NC	IO111NDB3	Rule 1
21	GFC1/IO126RSB1	GFC1/IO110PDB3	None
22	GFC0/IO125RSB1	GFC0/IO110NDB3	None
23	GFB1/IO124RSB1	GFB1/IO109PDB3	None
24	GFB0/IO123RSB1	GFB0/IO109NDB3	None
25	VCOMPLF	VCOMPLF	None
26	GFA0/IO122RSB1	GFA0/IO108NPB3	None
27	VCCPLF	VCCPLF	None
28	GFA1/IO121RSB1	GFA1/IO108PPB3	None
29	GND	GND	None
30	GFA2/IO120RSB1	GFA2/IO107PDB3	None
31	NC	IO107NDB3	Rule 1
32	GFB2/IO119RSB1	GFB2/IO106PDB3	None
33	NC	IO106NDB3	Rule 1

*Notes:*

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 7 • Pin Compatibility and Migration Table for ProASIC3 A3P125 and A3P250 with PQ208 Packaging (continued)**

Pin Number	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125
34	GFC2/IO118RSB1	GFC2/IO105PDB3	None
35	IO117RSB1	IO105NDB3	None
36	NC	NC	None
37	IO116RSB1	IO104PDB3	None
38	IO115RSB1	IO104NDB3	None
39	NC	IO103PSB3	Rule 1
40	VCCIB1	VCCIB3	Rule 5
41	GND	GND	None
42	IO114RSB1	IO101PDB3	None
43	IO113RSB1	IO101NDB3	None
44	GEC1/IO112RSB1	GEC1/IO100PDB3	None
45	GEC0/IO111RSB1	GEC0/IO100NDB3	None
46	GEB1/IO110RSB1	GEB1/IO99PDB3	None
47	GEB0/IO109RSB1	GEB0/IO99NDB3	None
48	GEA1/IO108RSB1	GEA1/IO98PDB3	None
49	GEA0/IO107RSB1	GEA0/IO98NDB3	None
50	VMV1	VMV3	Rule 5
51	GNDQ	GNDQ	None
52	GND	GND	None
53	NC	NC	None
54	NC	NC	None
55	GEA2/IO106RSB1	GEA2/IO97RSB2	None
56	GEB2/IO105RSB1	GEB2/IO96RSB2	None
57	GEC2/IO104RSB1	GEC2/IO95RSB2	None
58	IO103RSB1	IO94RSB2	None
59	IO102RSB1	IO93RSB2	None
60	IO101RSB1	IO92RSB2	None
61	IO100RSB1	IO91RSB2	None
62	VCCIB1	VCCIB2	Rule 5
63	IO99RSB1	IO90RSB2	None
64	IO98RSB1	IO89RSB2	None
65	GND	GND	None
66	IO97RSB1	IO88RSB2	None
67	IO96RSB1	IO87RSB2	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 7 • Pin Compatibility and Migration Table for ProASIC3 A3P125 and A3P250 with PQ208 Packaging (continued)**

Pin Number	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125
68	IO95RSB1	IO86RSB2	None
69	IO94RSB1	IO85RSB2	None
70	IO93RSB1	IO84RSB2	None
71	VCC	VCC	None
72	VCCIB1	VCCIB2	Rule 5
73	IO92RSB1	IO83RSB2	None
74	IO91RSB1	IO82RSB2	None
75	IO90RSB1	IO81RSB2	None
76	IO89RSB1	IO80RSB2	None
77	IO88RSB1	IO79RSB2	None
78	IO87RSB1	IO78RSB2	None
79	IO86RSB1	IO77RSB2	None
80	IO85RSB1	IO76RSB2	None
81	GND	GND	None
82	IO84RSB1	IO75RSB2	None
83	IO83RSB1	IO74RSB2	None
84	IO82RSB1	IO73RSB2	None
85	IO81RSB1	IO72RSB2	None
86	IO80RSB1	IO71RSB2	None
87	IO79RSB1	IO70RSB2	None
88	VCC	VCC	None
89	VCCIB1	VCCIB2	Rule 5
90	IO78RSB1	IO69RSB2	None
91	IO77RSB1	IO68RSB2	None
92	IO76RSB1	IO67RSB2	None
93	IO75RSB1	IO66RSB2	None
94	IO74RSB1	IO65RSB2	None
95	IO73RSB1	IO64RSB2	None
96	GDC2/IO72RSB1	GDC2/IO63RSB2	None
97	GND	GND	None
98	GDB2/IO71RSB1	GDB2/IO62RSB2	None
99	GDA2/IO70RSB1	GDA2/IO61RSB2	None
100	GNDQ	GNDQ	None
101	TCK	TCK	None

*Notes:*

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 7 • Pin Compatibility and Migration Table for ProASIC3 A3P125 and A3P250 with PQ208 Packaging (continued)**

Pin Number	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125
102	TDI	TDI	None
103	TMS	TMS	None
104	VMV1	VMV2	Rule 5
105	GND	GND	None
106	VPUMP	VPUMP	None
107	NC	NC	None
108	TDO	TDO	None
109	TRST	TRST	None
110	VJTAG	VJTAG	None
111	GDA0/IO66RSB0	GDA0/IO60VDB1	None
112	GDA1/IO65RSB0	GDA1/IO60UDB1	None
113	GDB0/IO64RSB0	GDB0/IO59VDB1	None
114	GDB1/IO63RSB0	GDB1/IO59UDB1	None
115	GDC0/IO62RSB0	GDC0/IO58VDB1	None
116	GDC1/IO61RSB0	GDC1/IO58UDB1	None
117	NC	IO57VDB1	Rule 1
118	NC	IO57UDB1	Rule 1
119	NC	IO56NDB1	Rule 1
120	NC	IO56PDB1	Rule 1
121	NC	IO55RSB1	Rule 1
122	GND	GND	None
123	VCCIB0	VCCIB1	Rule 5
124	NC	NC	None
125	NC	NC	None
126	VCC	VCC	None
127	IO60RSB0	IO53NDB1	None
128	GCC2/IO59RSB0	GCC2/IO53PDB1	None
129	GCB2/IO58RSB0	GCB2/IO52PSB1	None
130	GND	GND	None
131	GCA2/IO57RSB0	GCA2/IO51PSB1	None
132	GCA0/IO56RSB0	GCA1/IO50PDB1	None
133	GCA1/IO55RSB0	GCA0/IO50NDB1	None
134	GCB0/IO54RSB0	GCB0/IO49NDB1	None
135	GCB1/IO53RSB0	GCB1/IO49PDB1	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 7 • Pin Compatibility and Migration Table for ProASIC3 A3P125 and A3P250 with PQ208 Packaging (continued)**

Pin Number	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125
136	GCC0/IO52RSB0	GCC0/IO48NDB1	None
137	GCC1/IO51RSB0	GCC1/IO48PDB1	None
138	IO50RSB0	IO47NDB1	None
139	IO49RSB0	IO47PDB1	None
140	VCCIB0	VCCIB1	Rule 5
141	GND	GND	None
142	VCC	VCC	None
143	IO48RSB0	IO46RSB1	None
144	IO47RSB0	IO45NDB1	None
145	IO46RSB0	IO45PDB1	None
146	NC	IO44NDB1	Rule 1
147	NC	IO44PDB1	Rule 1
148	NC	IO43NDB1	Rule 1
149	GBC2/IO45RSB0	GBC2/IO43PDB1	None
150	IO44RSB0	IO42NDB1	None
151	GBB2/IO43RSB0	GBB2/IO42PDB1	None
152	IO42RSB0	IO41NDB1	None
153	GBA2/IO41RSB0	GBA2/IO41PDB1	None
154	VMV0	VMV1	Rule 5
155	GNDQ	GNDQ	None
156	GND	GND	None
157	NC	NC	None
158	GBA1/IO40RSB0	GBA1/IO40RSB0	None
159	GBA0/IO39RSB0	GBA0/IO39RSB0	None
160	GBB1/IO38RSB0	GBB1/IO38RSB0	None
161	GBB0/IO37RSB0	GBB0/IO37RSB0	None
162	GND	GND	None
163	GBC1/IO36RSB0	GBC1/IO36RSB0	None
164	GBC0/IO35RSB0	GBC0/IO35RSB0	None
165	IO34RSB0	IO34RSB0	None
166	IO33RSB0	IO33RSB0	None
167	IO32RSB0	IO32RSB0	None
168	IO31RSB0	IO31RSB0	None
169	IO30RSB0	IO30RSB0	None

*Notes:*

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 7 • Pin Compatibility and Migration Table for ProASIC3 A3P125 and A3P250 with PQ208 Packaging (continued)**

Pin Number	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125
170	VCCIB0	VCCIB0	None
171	VCC	VCC	None
172	IO29RSB0	IO29RSB0	None
173	IO28RSB0	IO28RSB0	None
174	IO27RSB0	IO27RSB0	None
175	IO26RSB0	IO26RSB0	None
176	IO25RSB0	IO25RSB0	None
177	IO24RSB0	IO24RSB0	None
178	GND	GND	None
179	IO23RSB0	IO23RSB0	None
180	IO22RSB0	IO22RSB0	None
181	IO21RSB0	IO21RSB0	None
182	IO20RSB0	IO20RSB0	None
183	IO19RSB0	IO19RSB0	None
184	IO18RSB0	IO18RSB0	None
185	IO17RSB0	IO17RSB0	None
186	VCCIB0	VCCIB0	None
187	VCC	VCC	None
188	IO16RSB0	IO16RSB0	None
189	IO15RSB0	IO15RSB0	None
190	IO14RSB0	IO14RSB0	None
191	IO13RSB0	IO13RSB0	None
192	IO12RSB0	IO12RSB0	None
193	IO11RSB0	IO11RSB0	None
194	IO10RSB0	IO10RSB0	None
195	GND	GND	None
196	IO09RSB0	IO09RSB0	None
197	IO08RSB0	IO08RSB0	None
198	IO07RSB0	IO07RSB0	None
199	IO06RSB0	IO06RSB0	None
200	VCCIB0	VCCIB0	None
201	GAC1/IO05RSB0	GAC1/IO05RSB0	None
202	GAC0/IO04RSB0	GAC0/IO04RSB0	None
203	GAB1/IO03RSB0	GAB1/IO03RSB0	None

*Notes:*

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 7 • Pin Compatibility and Migration Table for ProASIC3 A3P125 and A3P250 with PQ208 Packaging (continued)**

Pin Number	A3P125 Function	A3P250 Function	Migration Rule between A3P250 and A3P125
204	GAB0/IO02RSB0	GAB0/IO02RSB0	None
205	GAA1/IO01RSB0	GAA1/IO01RSB0	None
206	GAA0/IO00RSB0	GAA0/IO00RSB0	None
207	GNDQ	GNDQ	None
208	VMV0	VMV0	None

*Notes:*

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

## FG144 Package

**Table 8 • Pin Compatibility and Migration Table for ProASIC3 A3P060, A3P125, and A3P250 with FG144 Packaging**

Pin No.	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125
A1	GNDQ	GNDQ	GNDQ	None	None	None
A2	VMV0	VMV0	VMV0	None	None	None
A3	GAB0/IO04RSB0	GAB0/IO02RSB0	GAB0/IO02RSB0	None	None	None
A4	GAB1/IO05RSB0	GAB1/IO03RSB0	GAB1/IO03RSB0	None	None	None
A5	IO08RSB0	IO11RSB0	IO16RSB0	None	None	None
A6	GND	GND	GND	None	None	None
A7	IO11RSB0	IO18RSB0	IO29RSB0	None	None	None
A8	VCC	VCC	VCC	None	None	None
A9	IO16RSB0	IO25RSB0	IO33RSB0	None	None	None
A10	GBA0/IO23RSB0	GBA0/IO39RSB0	GBA0/IO39RSB0	None	None	None
A11	GBA1/IO24RSB0	GBA1/IO40RSB0	GBA1/IO40RSB0	None	None	None
A12	GNDQ	GNDQ	GNDQ	None	None	None
B1	GAB2/IO53RSB1	GAB2/IO69RSB1	GAB2/IO117UDB3	None	None	None
B2	GND	GND	GND	None	None	None
B3	GAA0/IO02RSB0	GAA0/IO00RSB0	GAA0/IO00RSB0	None	None	None
B4	GAA1/IO03RSB0	GAA1/IO01RSB0	GAA1/IO01RSB0	None	None	None
B5	IO00RSB0	IO08RSB0	IO14RSB0	None	None	None
B6	IO10RSB0	IO14RSB0	IO19RSB0	None	None	None
B7	IO12RSB0	IO19RSB0	IO22RSB0	None	None	None
B8	IO14RSB0	IO22RSB0	IO30RSB0	None	None	None
B9	GBB0/IO21RSB0	GBB0/IO37RSB0	GBB0/IO37RSB0	None	None	None
B10	GBB1/IO22RSB0	GBB1/IO38RSB0	GBB1/IO38RSB0	None	None	None
B11	GND	GND	GND	None	None	None
B12	VMV0	VMV0	VMV1	None	None	None
C1	IO95RSB1	IO132RSB1	IO117VDB3	None	None	None
C2	GFA2/IO83RSB1	GFA2/IO120RSB1	GFA2/IO107PPB3	None	None	None
C3	GAC2/IO94RSB1	GAC2/IO131RSB1	GAC2/IO116UDB3	None	None	None
C4	VCC	VCC	VCC	None	None	None
C5	IO01RSB0	IO10RSB0	IO12RSB0	None	None	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 8 • Pin Compatibility and Migration Table for ProASIC3 A3P060, A3P125, and A3P250 with FG144 Packaging (continued)**

Pin No.	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125
C6	IO09RSB0	IO12RSB0	IO17RSB0	None	None	None
C7	IO13RSB0	IO21RSB0	IO24RSB0	None	None	None
C8	IO15RSB0	IO24RSB0	IO31RSB0	None	None	None
C9	IO17RSB0	IO27RSB0	IO34RSB0	None	None	None
C10	GBA2/IO25RSB0	GBA2/IO41RSB0	GBA2/IO41PDB1	None	None	None
C11	IO26RSB0	IO42RSB0	IO41NDB1	None	None	None
C12	GBC2/IO29RSB0	GBC2/IO45RSB0	GBC2/IO43PPB1	None	None	None
D1	IO91RSB1	IO128RSB1	IO112NDB3	None	None	None
D2	IO92RSB1	IO129RSB1	IO112PDB3	None	None	None
D3	IO93RSB1	IO130RSB1	IO116VDB3	None	None	None
D4	GAA2/IO51RSB1	GAA2/IO67RSB1	GAA2/IO118UPB3	None	None	None
D5	GAC0/IO06RSB0	GAC0/IO04RSB0	GAC0/IO04RSB0	None	None	None
D6	GAC1/IO07RSB0	GAC1/IO05RSB0	GAC1/IO05RSB0	None	None	None
D7	GBC0/IO19RSB0	GBC0/IO35RSB0	GBC0/IO35RSB0	None	None	None
D8	GBC1/IO20RSB0	GBC1/IO36RSB0	GBC1/IO36RSB0	None	None	None
D9	GBB2/IO27RSB0	GBB2/IO43RSB0	GBB2/IO42PDB1	None	None	None
D10	IO18RSB0	IO28RSB0	IO42NDB1	None	None	None
D11	IO28RSB0	IO44RSB0	IO43NPB1	None	None	None
D12	GCB1/IO37RSB0	GCB1/IO53RSB0	GCB1/IO49PPB1	None	None	None
E1	VCC	VCC	VCC	None	None	None
E2	GFC0/IO88RSB1	GFC0/IO125RSB1	GFC0/IO110NDB3	None	None	None
E3	GFC1/IO89RSB1	GFC1/IO126RSB1	GFC1/IO110PDB3	None	None	None
E4	VCCIB1	VCCIB1	VCCIB3	None	Rule 5	Rule 5
E5	IO52RSB1	IO68RSB1	IO118VPB3	None	None	None
E6	VCCIB0	VCCIB0	VCCIB0	None	None	None
E7	VCCIB0	VCCIB0	VCCIB0	None	None	None
E8	GCC1/IO35RSB0	GCC1/IO51RSB0	GCC1/IO48PDB1	None	None	None
E9	VCCIB0	VCCIB0	VCCIB1	None	Rule 5	Rule 5
E10	VCC	VCC	VCC	None	None	None
E11	GCA0/IO40RSB0	GCA0/IO56RSB0	GCA0/IO50NDB1	None	None	None
E12	IO30RSB0	IO46RSB0	IO51NDB1	None	None	None

*Notes:*

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 8 • Pin Compatibility and Migration Table for ProASIC3 A3P060, A3P125, and A3P250 with FG144 Packaging (continued)**

Pin No.	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125
F1	GFB0/IO86RSB1	GFB0/IO123RSB1	GFB0/IO109NPB3	None	None	None
F2	VCOMPLF	VCOMPLF	VCOMPLF	None	None	None
F3	GFB1/IO87RSB1	GFB1/IO124RSB1	GFB1/IO109PPB3	None	None	None
F4	IO90RSB1	IO127RSB1	IO107NPB3	None	None	None
F5	GND	GND	GND	None	None	None
F6	GND	GND	GND	None	None	None
F7	GND	GND	GND	None	None	None
F8	GCC0/IO36RSB0	GCC0/IO52RSB0	GCC0/IO48NDB1	None	None	None
F9	GCB0/IO38RSB0	GCB0/IO54RSB0	GCB0/IO49NPB1	None	None	None
F10	GND	GND	GND	None	None	None
F11	GCA1/IO39RSB0	GCA1/IO55RSB0	GCA1/IO50PDB1	None	None	None
F12	GCA2/IO41RSB0	GCA2/IO57RSB0	GCA2/IO51PDB1	None	None	None
G1	GFA1/IO84RSB1	GFA1/IO121RSB1	GFA1/IO108PPB3	None	None	None
G2	GND	GND	GND	None	None	None
G3	VCCPLF	VCCPLF	VCCPLF	None	None	None
G4	GFA0/IO85RSB1	GFA0/IO122RSB1	GFA0/IO108NPB3	None	None	None
G5	GND	GND	GND	None	None	None
G6	GND	GND	GND	None	None	None
G7	GND	GND	GND	None	None	None
G8	GDC1/IO45RSB0	GDC1/IO61RSB0	GDC1/IO58UPB1	None	None	None
G9	IO32RSB0	IO48RSB0	IO53NDB1	None	None	None
G10	GCC2/IO43RSB0	GCC2/IO59RSB0	GCC2/IO53PDB1	None	None	None
G11	IO31RSB0	IO47RSB0	IO52NDB1	None	None	None
G12	GCB2/IO42RSB0	GCB2/IO58RSB0	GCB2/IO52PDB1	None	None	None
H1	VCC	VCC	VCC	None	None	None
H2	GFB2/IO82RSB1	GFB2/IO119RSB1	GFB2/IO106PDB3	None	None	None
H3	GFC2/IO81RSB1	GFC2/IO118RSB1	GFC2/IO105PSB3	None	None	None
H4	GEC1/IO77RSB1	GEC1/IO112RSB1	GEC1/IO100PDB3	None	None	None
H5	VCC	VCC	VCC	None	None	None
H6	IO34RSB0	IO50RSB0	IO79RSB2	None	None	None
H7	IO44RSB0	IO60RSB0	IO65RSB2	None	None	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 8 • Pin Compatibility and Migration Table for ProASIC3 A3P060, A3P125, and A3P250 with FG144 Packaging (continued)**

Pin No.	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125
H8	GDB2/IO55RSB1	GDB2/IO71RSB1	GDB2/IO62RSB2	None	None	None
H9	GDC0/IO46RSB0	GDC0/IO62RSB0	GDC0/IO58VPB1	None	None	None
H10	VCCIB0	VCCIB0	VCCIB1	None	Rule 5	Rule 5
H11	IO33RSB0	IO49RSB0	IO54PSB1	None	None	None
H12	VCC	VCC	VCC	None	None	None
J1	GEB1/IO75RSB1	GEB1/IO110RSB1	GEB1/IO99PDB3	None	None	None
J2	IO78RSB1	IO115RSB1	IO106NDB3	None	None	None
J3	VCCIB1	VCCIB1	VCCIB3	None	Rule 5	Rule 5
J4	GEC0/IO76RSB1	GEC0/IO111RSB1	GEC0/IO100NDB3	None	None	None
J5	IO79RSB1	IO116RSB1	IO88RSB2	None	None	None
J6	IO80RSB1	IO117RSB1	IO81RSB2	None	None	None
J7	VCC	VCC	VCC	None	None	None
J8	TCK	TCK	TCK	None	None	None
J9	GDA2/IO54RSB1	GDA2/IO70RSB1	GDA2/IO61RSB2	None	None	None
J10	TDO	TDO	TDO	None	None	None
J11	GDA1/IO49RSB0	GDA1/IO65RSB0	GDA1/IO60UDB1	None	None	None
J12	GDB1/IO47RSB0	GDB1/IO63RSB0	GDB1/IO59UDB1	None	None	None
K1	GEB0/IO74RSB1	GEB0/IO109RSB1	GEB0/IO99NDB3	None	None	None
K2	GEA1/IO73RSB1	GEA1/IO108RSB1	GEA1/IO98PDB3	None	None	None
K3	GEA0/IO72RSB1	GEA0/IO107RSB1	GEA0/IO98NDB3	None	None	None
K4	GEA2/IO71RSB1	GEA2/IO106RSB1	GEA2/IO97RSB2	None	None	None
K5	IO65RSB1	IO100RSB1	IO90RSB2	None	None	None
K6	IO64RSB1	IO98RSB1	IO84RSB2	None	None	None
K7	GND	GND	GND	None	None	None
K8	IO57RSB1	IO73RSB1	IO66RSB2	None	None	None
K9	GDC2/IO56RSB1	GDC2/IO72RSB1	GDC2/IO63RSB2	None	None	None
K10	GND	GND	GND	None	None	None
K11	GDA0/IO50RSB0	GDA0/IO66RSB0	GDA0/IO60VDB1	None	None	None
K12	GDB0/IO48RSB0	GDB0/IO64RSB0	GDB0/IO59VDB1	None	None	None
L1	GND	GND	GND	None	None	None
L2	VMV1	VMV1	VMV3	None	Rule 5	Rule 5

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

**Table 8 • Pin Compatibility and Migration Table for ProASIC3 A3P060, A3P125, and A3P250 with FG144 Packaging (continued)**

Pin No.	A3P060 Function	A3P125 Function	A3P250 Function	Migration Rule between A3P125 and A3P060	Migration Rule between A3P250 and A3P060	Migration Rule between A3P250 and A3P125
L3	GEB2/IO70RSB1	GEB2/IO105RSB1	GEB2/IO96RSB2	None	None	None
L4	IO67RSB1	IO102RSB1	IO91RSB2	None	None	None
L5	VCCIB1	VCCIB1	VCCIB2	None	Rule 5	Rule 5
L6	IO62RSB1	IO95RSB1	IO82RSB2	None	None	None
L7	IO59RSB1	IO85RSB1	IO80RSB2	None	None	None
L8	IO58RSB1	IO74RSB1	IO72RSB2	None	None	None
L9	TMS	TMS	TMS	None	None	None
L10	VJTAG	VJTAG	VJTAG	None	None	None
L11	VMV1	VMV1	VMV2	None	Rule 5	Rule 5
L12	TRST	TRST	TRST	None	None	None
M1	GNDQ	GNDQ	GNDQ	None	None	None
M2	GEC2/IO69RSB1	GEC2/IO104RSB1	GEC2/IO95RSB2	None	None	None
M3	IO68RSB1	IO103RSB1	IO92RSB2	None	None	None
M4	IO66RSB1	IO101RSB1	IO89RSB2	None	None	None
M5	IO63RSB1	IO97RSB1	IO87RSB2	None	None	None
M6	IO61RSB1	IO94RSB1	IO85RSB2	None	None	None
M7	IO60RSB1	IO86RSB1	IO78RSB2	None	None	None
M8	NC	IO75RSB1	IO76RSB2	Rule 1	Rule 1	None
M9	TDI	TDI	TDI	None	None	None
M10	VCCIB1	VCCIB1	VCCIB2	None	Rule 5	Rule 5
M11	VPUMP	VPUMP	VPUMP	None	None	None
M12	GNDQ	GNDQ	GNDQ	None	None	None

**Notes:**

1. See [Table 3 on page 3](#) for the high-density/low-density pin combination guidelines.
2. "None" implies that the pins can be connected without any change.

## Conclusion

This application note describes the design migration among ProASIC3 family devices with an emphasis on package pin compatibility. Devices in the ProASIC3 family share numerous common architectural features. However, not all architectural features of family members are identical; use the datasheet to identify differences. Additionally, a key requirement is running functional simulation before and after the migration using Microsemi tools. Microsemi will continue to update this document with additional packages.



<b>Date</b>	<b>Changes</b>	<b>Page</b>
51900135-1/12.06	QN132 information was added to <a href="#">Table 1 • Device Information</a> .	1
	QN132 information was added to <a href="#">Table 2 • Common and Convertible I/Os</a> .	2
	<a href="#">Table 6 • Pin Compatibility and Migration Table for ProASIC3 A3P060 and A3P125 with TQ144 Packaging</a> is new.	16



**Microsemi Corporate Headquarters**  
One Enterprise, Aliso Viejo CA 92656 USA  
Within the USA: +1 (949) 380-6100  
Sales: +1 (949) 380-6136  
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at [www.microsemi.com](http://www.microsemi.com).

---

© 2011 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.