42MX Family Devices Power-Up Behavior

Introduction

Actel antifuse FPGA families offer the advantage of nonvolatility by attaining immediate functionality at power-up. Since the programmed design is retained, there is no requirement for additional configuration devices. This application note discusses the results of the 42MX device power-up characterization in detail and recommends appropriate power-up sequences and ramp-rates. Tristate behavior of the device I/Os during the power-up cycle offers the flexibility of applying voltages to the I/Os during power-up.

The characterization measurement was performed in a laboratory environment and the reported data is typical. Hence, the maximum and minimum values under best and worst condition are not guaranteed.

Background

For 42MX devices manufactured before April 1999, the I/Os would go incorrectly into tristate mode under certain power-up conditions. In an effort to resolve this problem, Actel has created an updated set of 42MX devices, designated by "X39" in their part number. For more information, refer to the following GURU documents:

http://www.actel.com/apps/guru/apr99/ns845.html

http://www.actel.com/apps/guru/jul99/ns842.html

This application note includes the characterization reports for both old and new versions of the 42MX family, and is a general source for all 42MX devices.

All 42MX devices have two power supplies: V_{CCA} and V_{CCI}. They can operate in 5 V only, 3.3 V only, and 5 V / 3.3 V mixed systems. Table 1 summarizes the voltage levels of these power supplies and the corresponding I/O voltage level.

Table 1 • **Power Supply Levels for Different Operations**

V_{CCA}	V_{CCI}	Input	Output
5 V	5 V	5 V	5 V
3.3 V	3.3 V	3.3 V	3.3 V
5 V	3.3 V	3.3 V, 5 V	3.3 V

As seen from Table 1, V_{CCA} also acts as an input tolerance voltage while V_{CCI} is used as an I/O module voltage. In single voltage operations, V_{CCA} and V_{CCI} are usually tied to each other, but for the mixed 5 V / 3.3 V systems (V_{CCA} = 5 V and V_{CCI} = 3.3 V), V_{CCA} must be greater than or equal to V_{CCI} throughout the power-up sequence. Hence, V_{CCA} must always be powered up before V_{CCI} to avoid excessive currents and/ or damage to the device.

If V_{CCI} is 0.5 V greater than V_{CCA} when both are above 1.5 V, then the input protection junction on the I/Os will be forward biased, causing them to draw large amounts of current. When V_{CCA} and V_{CCI} are in the 1.5 V to 2.0 V region, and V_{CCI} is greater than V_{CCA}, all I/Os would momentarily behave as outputs that are in a logical high state, and I_{CC} rises to high levels.

The A42MX24 and A42MX36 devices contain an internal power-on reset (POR) circuitry used to reset the JTAG state machine. Actel recommends that V_{CCA} is monotonic in order for the POR to issue a proper JTAG reset. If V_{CCA} is not monotonic, the internal JTAG POR may not operate as expected. In this case, the device may enter a JTAG test mode after power-up instead of the normal operation mode. The JTAG state machine can be reset externally using any of the following methods:

- After power-up, issue at least five TCK cycles with TMS pulled high.
- If JTAG is not used in the design, JTAG can be permanently disabled by clearing the check box for the **Reserve JTAG** pin option in Designer. This causes the JTAG state machine to remain in an asynchronous reset state, bypassing the POR. However, note that in this case the JTAG circuitry is permanently disabled and JTAG testing cannot be performed on the device.

Transient Current

Due to the simultaneous random logic switching activity during power-up, a relatively large transient current may appear on the core supply (V_{CCA}). The amount and duration of the transient current is dependent on the V_{CCA} voltage level (3.3 V or 5 V) and its ramp-rate during power-up. Since the transient current is not due to I/O switching, its value and duration are independent of the V_{CCI} level.

Transient current measurements are taken for three different operating conditions:

- 5 V only: $V_{CCA} = V_{CCI} = 5$ V
- 3.3 V only: $V_{CCA} = V_{CCI} = 3.3$ V
- Mixed 5 V / 3.3 V: $V_{CCA} = 5$ V (powered up first), $V_{CCI} = 3.3$ V (powered up second)

Different ramp-rates have been applied to the power supplies. Additionally, in the mixed-voltage operating conditions, different delays between V_{CCA} and V_{CCI} have been tested, ranging from 100 µs to 250 ms. Table 2 and Table 3 indicate the amount of the transient current peak in single-voltage operating conditions for the X39 and non-X39 series, respectively.

The average pulse width of the transient current spike, which can be derived from the measured data, is 350 ns, with its value increasing as the power supply ramp-rate increases. The transient current peak value is also related to the number of logic modules in the device, meaning that larger devices show a higher transient current. For instance, for all of the X39 series tested devices, A42MX36 has a higher transient current than A42MX24, which in turn, has a higher transient current than A42MX16. However, for the non-X39 measured devices, some discrepancies can be observed. These discrepancies can be seen in Table 2 and Table 3.

The transient currents were reduced with the slower ramp-rates. Figure 1 on page 3 shows the relation between the ramp-rates and the transient current peak for the X39 series of 42MX family devices.

For mixed-voltage systems, the transient current is very similar to that of the 5-V-only operation.

Table 2 • **Transient Current for X39 42MX Parts at Different Ramp-Rates**

Operating Systems	Products	Transient Current on V_{CCA} (mA) at Different Ramp-Rates (average values)						
		0.5 V / µs	**0.05 V / µs**	**10 V / ms**	**5 V / ms**	**0.5 V / ms**	**0.2 V / ms**	**0.05 V / ms**
5-V-only systems	A42MX16 X39	428	319	255	165	101	95	92
	A42MX24 X39	490	465	340	250	130	108	110
	A42MX36 X39	539	531	357	346	151	117	112
		Transient Current on V_{CCA} (mA) at Different Ramp-Rates (average values)						
3.3-V-only systems	**Products**	**0.33 V / µs**	**0.033 V / µs**	**6.6 V / ms**	**3.3 V / ms**	**0.33 V / ms**	**0.132 V / ms**	**0.033 V / ms**
	A42MX16 X39	196	189	183	148	97	95	90
	A42MX24 X39	281	276	265	216	129	113	107
	A42MX36 X39	324	327	321	284	124	112	110

Table 3 • **Transient Current for Non-X39 42MX Parts at Different Ramp-Rates**

Operating Systems	Products	Transient Current on V_{CCA} (mA) at Different Ramp-Rates (average values)						
		0.5 V / µs	**0.05 V / µs**	**10 V / ms**	**5 V / ms**	**0.5 V / ms**	**0.2 V / ms**	**0.05 V / ms**
5-V-only systems	A42MX16	N/A	N/A	189	140	47	45	43
	A42MX24	N/A	N/A	250	234	202	200	197
	A42MX36	N/A	N/A	78	64	56	117	108
3.3-V-only systems		**Transient Current on V_{CCA} (mA) at Different Ramp-Rates (average values)**						
	Products	**0.33 V / µs**	**0.033 V / µs**	**6.6 V / ms**	**3.3 V / ms**	**0.33 V / ms**	**0.132 V / ms**	**0.033 V / ms**
	A42MX16	184	171	150	114	50	49	85
	A42MX24	225	220	208	207	205	199	197
	A42MX36	159	89	70	65	55	114	112

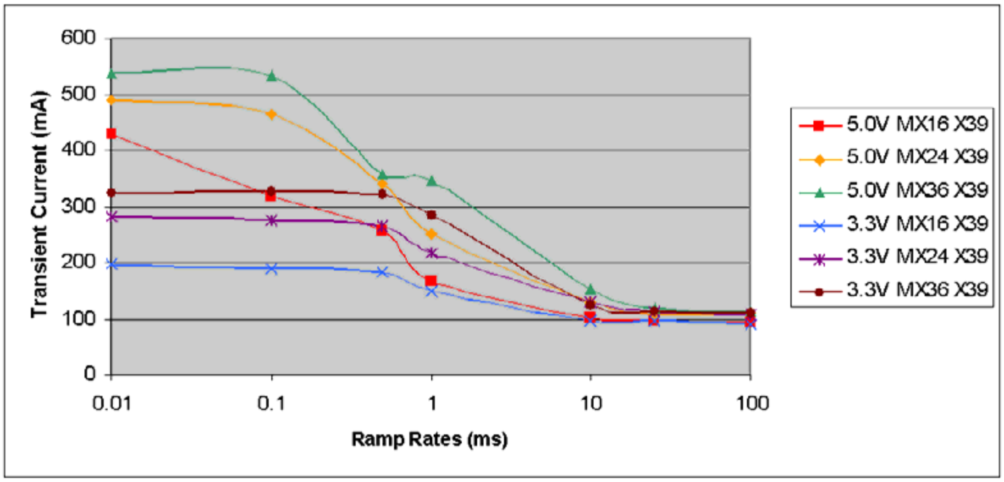

Figure 1 • **Transient Current vs. Ramp-Rates for A42MX16, A42MX24, and A42MX36 at 5 V and 3.3 V Operating Conditions**

I/O Behavior During Power-Up

This section discusses the behavior of 42MX device family I/Os during power-up cycles. One of the important parameters during power-up is the voltage level at which the I/Os become functional. Since the functionality of I/Os is defined by the time the internal logic is functional, the power-up to functional time depends on the ramp-rates of V_{CCA} and not V_{CCI}. However, the proper data cannot be read from or written into the device unless V_{CCI} reaches the value where I/Os become active. After the I/Os become active, there will be some additional delay for the input data to propagate to the output pins. In single-voltage operations, there is only one power supply. Therefore, the power-up to functional times and I/O functional times are equal. Table 4 and Table 5 present the power-up to functional voltage levels for the single-voltage operation mode. The two tables also indicate the amount that the power-up to functional voltage level increases for faster ramp-rates and larger arrays.

Table 4 • **V_{CCA} Voltage Where I/Os Become Active in 5-V-Only Operation (V)**

Ramp-Rate	0.5 V / µs	0.05 V / µs	10 V / ms	5 V / ms	0.5 V / ms	0.2 V / ms	0.05 V / ms
A42MX16 X39	5.00	4.65	3.13	2.81	2.41	2.31	2.25
A42MX24 X39	5.00	4.81	3.63	3.16	2.41	2.40	2.34
A42MX36 X39	5.00	4.91	3.92	3.73	2.54	2.38	2.36
A42MX16	N/A	N/A	3.51	2.87	1.90	1.77	1.73
A42MX24	N/A	N/A	3.53	3.00	2.55	2.50	2.49
42MX36	N/A	N/A	1.96	1.94	1.86	2.41	2.38

Table 5 • **V_{CCA} Voltage Where I/Os Become Active in 3.3-V-Only Operation (V)**

Ramp-Rate	0.33 V / µs	0.033 V / µs	6.6 V / ms	3.3 V / ms	0.33 V / ms	0.132 V / ms	0.033 V / ms
A42MX16 X39	3.30	3.30	2.88	2.66	2.33	2.30	2.25
A42MX24 X39	3.30	3.30	3.19	2.93	2.40	2.34	2.28
A42MX36 X39	3.30	3.30	3.30	3.07	2.46	2.41	2.34
A42MX16	3.30	3.30	3.01	3.67	1.78	1.76	1.65
A42MX24	3.30	3.30	3.11	2.70	2.47	2.43	2.43
A42MX36	2.53	2.07	1.91	1.82	1.79	2.38	2.38

In a mixed-voltage operation mode, since the array voltage (V_{CCA}) is 5 V, and the power-up to functional time depends on the V_{CCA} ramp-up, Table 4 on page 3 applies for mixed-voltage mode. However, there are two cases that should be taken into consideration during the power-up in a mixed-voltage mode. The first case occurs when the power-up delay between V_{CCA} and V_{CCI} is larger than the power-up to functional time. In this case, the internal modules are functional and the I/Os are inactive. Therefore, each I/O's functional time will be defined as the time when V_{CCI} is powered up. The second case is more critical and happens if the power-up delay between V_{CCA} and V_{CCI} is less than the power-up to functional time. In other words, it happens when the I/Os are functional but the internal logic modules are not. Thus, the I/Os will be driven to their designated voltage level as soon as the power-up to functional time is reached. In such a condition, there is a short period of time (after I/O activation and before array functionality) that the I/Os might be driven into an unknown state. Hence, Actel recommends to power-up V_{CCI} after V_{CCA} has reached its functional level.

During the characterization procedure, the inputs and outputs of 42MX family devices are tested to determine their behavior during power-up, specifically before they become functional. The results of different measurements demonstrate that the I/Os are tristated during the power-up. In other words, a voltage can be applied to a 42MX device I/O before and during power-up of the device.

Users should note that for non-X39 devices in 5-V-only operation, if the power-up ramp-rate of V_{CCI} is faster than 0.01 V/µs, the I/Os will be driven into an unknown tristate mode, and the device will not function properly.

Conclusion

For proper power-up of 42MX family devices, V_{CCA} should always be greater than V_{CCI} during power-up. In older generations (non-X39) of the 42MX family, there is a power-up rise time restriction to avoid an incorrect tristate on I/Os. This document discussed the transient current on V_{CCA} and the functional voltage level during power-up. The transient current in 42MX devices is reduced by increasing the power-up rise time. For faster power-up, the voltage level in which the device becomes functional is higher. 42MX device I/Os are also tristated before reaching the functionality point, which makes it possible to apply voltage on I/Os during power-up.

List of Changes

Previous Version	Changes in Current Version 5192696-3/10.06*	Page
5192696-2/3.05	The "Background" section was updated.	1
5192696-1/3.03	"Transient Current" was updated.	2

Note: * The part number is located on the last page of the document.

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