
Level Shifter Design Example

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General Description

Semiconductor technology advancements, proliferating I/O standards, legacy support requirements, and the relentless drive to design and manufacture lower power systems require most applications to utilize a mix of power supply and I/O drive voltages. Today's lower power devices have to work in this eco-system with the older, higher voltage devices, requiring solutions that interface with the multiple voltages that are in widespread use today.

Level-translator integrated circuits (ICs) are a common solution, but they do not necessarily provide the flexibility to support multiple simultaneous translations to different voltages or I/O interface standard. Level-translator ICs can add unnecessary cost if the system already contains an FPGA on board. This level shifter design example provides a low-cost, low-power, highly flexible solution that utilizes Actel IGLOO[®] low-power FPGAs.

Design Description

All Actel IGLOO and ProASIC[®]3 low-power FPGAs support multiple voltage options for I/O banks. The VCCI of each bank determines the voltage level of its I/Os. Within the IGLOO series of FPGAs, I/O voltages are available from 1.2 V up to 3.3 V, including several flexible wide range I/O voltage options.

This design example is based on the IGLOO starter kit board (part number AGL-DEV-KIT-SCS), although the design and instructions can be easily adapted to work with any of the Actel IGLOO or ProASIC3 boards. A full list of available boards can be found on the Actel website (www.actel.com).

Design files can be downloaded from the Actel website:
www.actel.com/download/rsc/?f=LevelShifter_DF.

Level Shifter Design Example

Figure 1 shows the provision for selecting I/O bank VCCI voltages on the IGLOO starter kit by using jumpers. Bank1 can use an I/O voltage of 3.3 V or 1.5 V. Bank2 can use an I/O voltage of 2.5 V or 1.5 V.

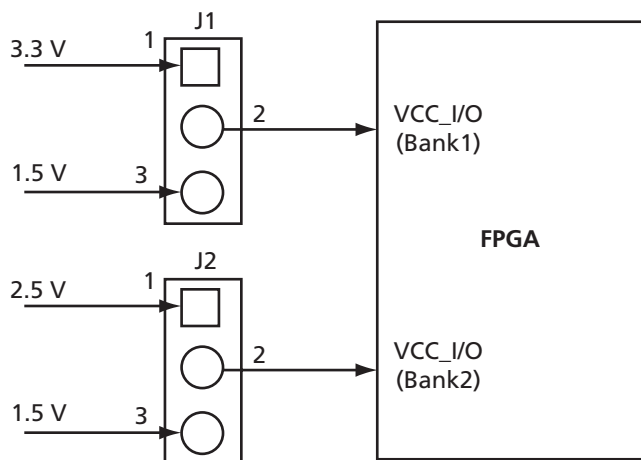


Figure 1 • Jumper Setting

Top-Level Block Diagram

The logic in this design example is the straightforward passing of data from inputs on one voltage bank to outputs on another voltage bank (Figure 2).

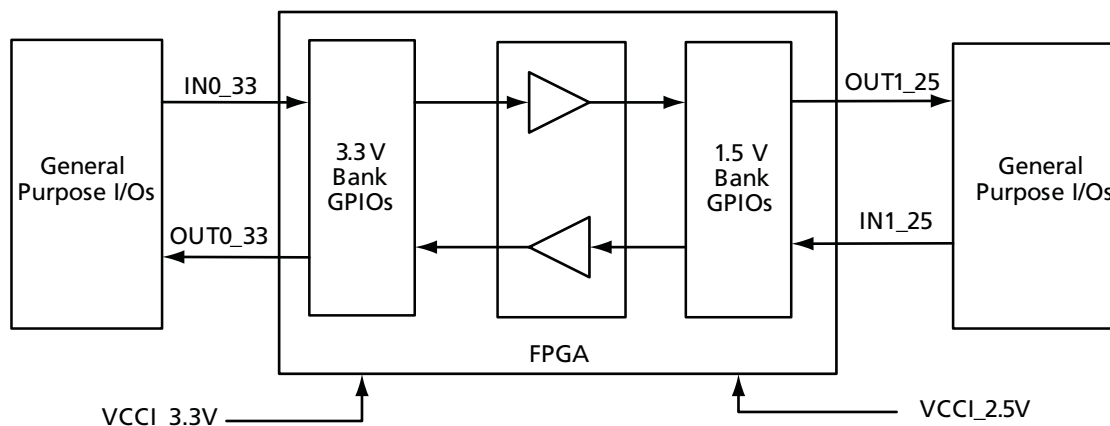


Figure 2 • System Block Diagram

The design does not consume any other logic than the routing resources and I/Os.

Interface Description

Table 1 describes the interconnections between the ports and the I/Os.

Table 1 • Signal Description

Port	Direction	Description
IN1_25	I	2.5 V input connected to Bank1
INO_33	I	3.3 V input connected to Bank0
OUT1_25	O	2.5 V output connected to Bank1
OUT0_33	O	3.3 V output connected to Bank0

Utilization Details

For testing purposes, this design was created for the M1AGL600V2-484FBGA device. Table 2 describes the utilization details after place-and-route.

Table 2 • Utilization Details

Resource	Utilized	Total	Percentage
Core	0	13,824	0.00 %
I/Os	4	235	1.70%
Differential I/Os	0	60	0.00%
GLOBAL (chip + quadrant)	0	18	0.00 %
PLL	0	1	0.00 %
RAM/FIFO	0	24	0.00 %
Low Static ICC	0	1	0.00 %
FlashROM	0	1	0.00 %
User JTAG	0	1	0.00 %

Testing Scheme

This design was tested and verified on the M1AGL600V2 development kit. In this board, the VCCI for Bank0 is 3.3 V and 2.5 V for Bank1.

For verifying the functionality of the IP, an external clock source of 2.5 V amplitude was connected to one of the pins of Bank1. The logic within the FPGA connects this pin to one of the pins of Bank0. Table 3 shows the connectivity details.

Table 3 • Details of 2.5 V to 3.3 V Conversion

Signal Name	Direction	Bank / VCCI	FPGA Pin Number	Board Reference	Voltage Measured
IN1_2.5	Input	Bank1 / 2.5 V	H16	P2 Pin No.4	2.5 V
OUT0_33	Output	Bank0 / 3.3 V	D5	P1 Pin No. 4	3.3 V

The voltage level translation, from 2.5 V to 3.3 V, is shown in Figure 3 on page 4.

Timing Diagrams

Figure 3 shows the timing diagram for the 2.5 V to 3.3 V translation.

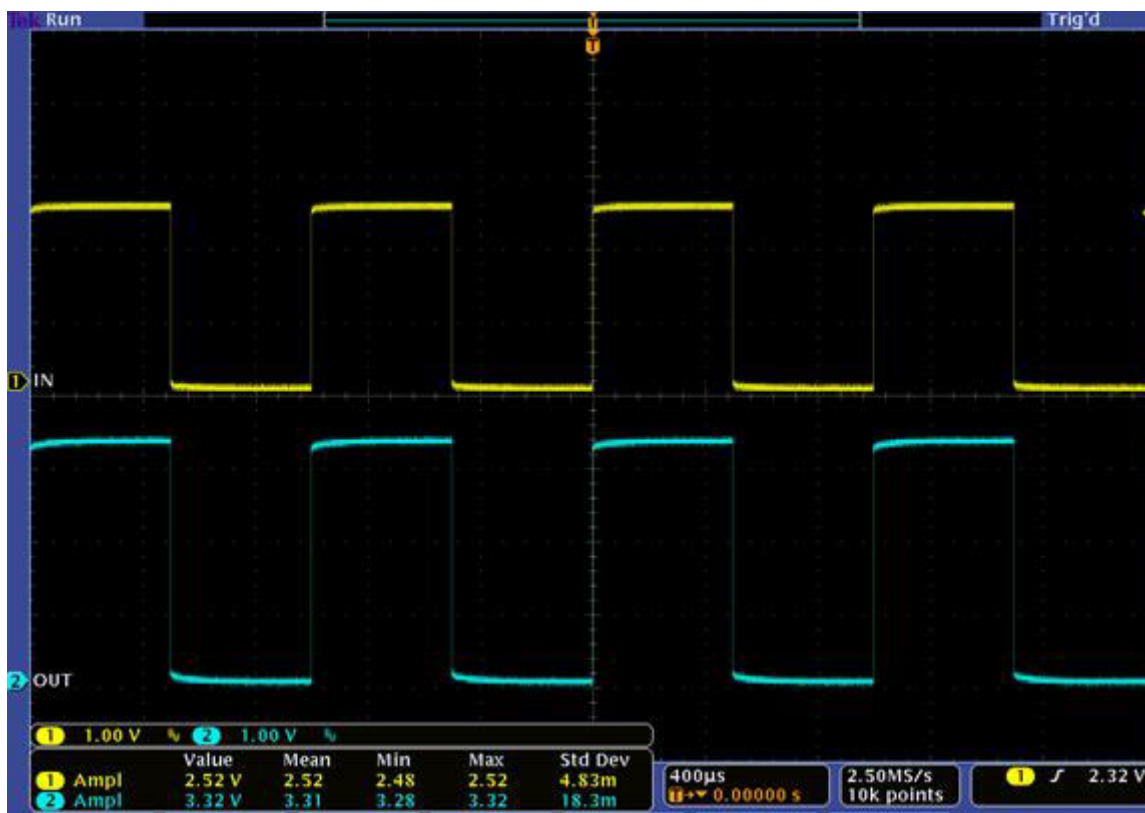


Figure 3 • Translating from 2.5 V to 3.3 V

Another sets of pins were used for the 3.3 V to 2.5 V conversion. The connectivity details are shown in Table 4.

Table 4 • Details of 3.3 V to 2.5 V Conversion

Signal Name	Direction	Bank / VCCI	FPGA Pin Number	Board Reference	Voltage Measured
IN0_33	Input	Bank0 / 3.3 V	D10	P1 Pin No. 6	3.3 V
OUT1_25	Output	Bank1 / 2.5 V	J16	P2 Pin No. 35	2.5 V

Figure 4 shows the resulting waveform.

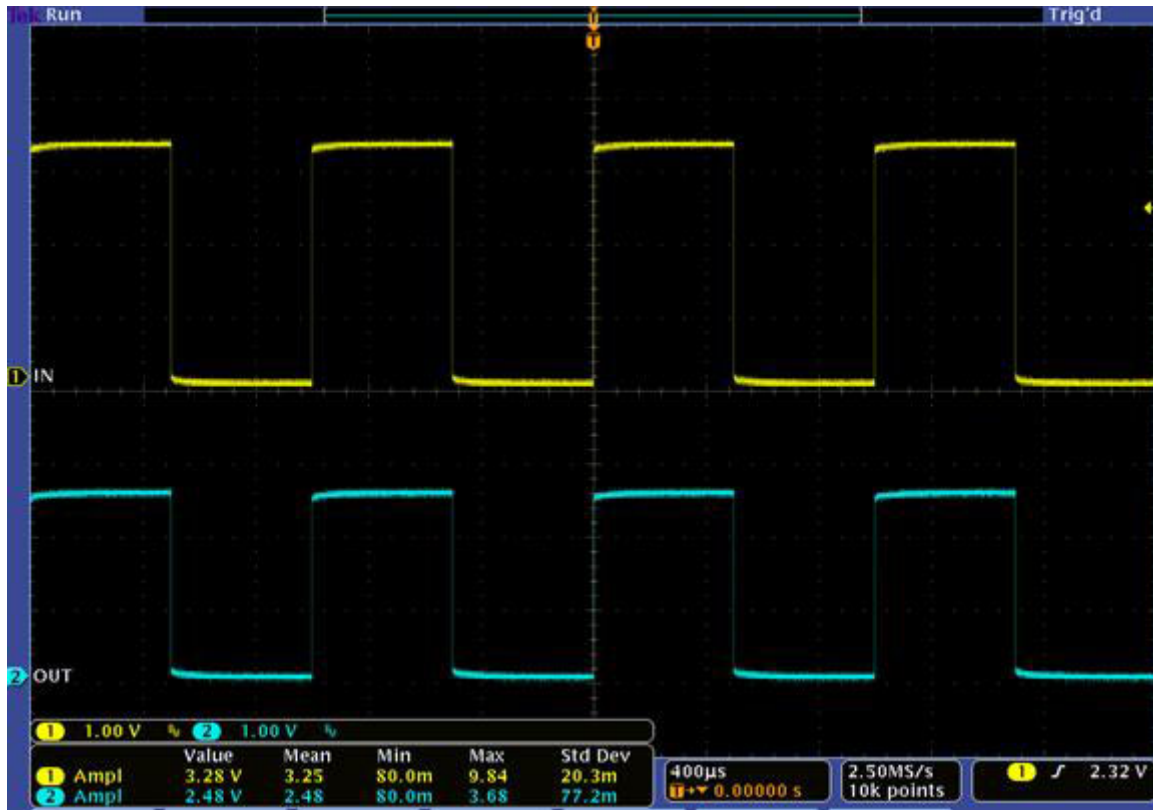


Figure 4 • Translating from 3.3 V to 2.5 V

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