Global Clock Networks in Actel Antifuse Devices

System performance is one of the most important characteristics of a design. As a result, designers put a lot of effort into improving clock speed. Clock skew is often a limiting factor in attaining maximum performance, forcing designers to slow down their designs to avoid setup and hold-time violations. High fanout can also limit the timing performance of designs. Regardless of the efficiency of a coding style, the clock skew and signal fanout put a physical limitation on the speed of the design. The Actel architecture provides global clock networks that allow high-fanout drive for registers, with little or no delay penalty and minimal skew. These networks enable the entire device to be spanned with fast, low-skew routing resources.

The low-skew clock networks can be driven by internally-generated signals or non-clock high fanout signals through regular I/O pins. Combining this flexibility with the efficiency of low-skew networks allows designers to achieve very high speeds without compromising their original designs.

Clock Network Resources

Actel's antifuse device families provide different global clock network resources, each of which provides certain advantages for the user in improving his/her design. Knowing these advantages and considering the design requirements will help the designer select the most efficient device family in terms of clocking speed.

Dedicated Clock Network

The dedicated hardwired clock (HCLK) network is directly wired from the HCLK input pin to the clock inputs of sequential cells. There are no programming elements in the path from the I/O pad driver to the inputs of S-modules. This provides a fast propagation route for input clock signals, enabling very fast clock-to-out performance and negligible clock skew (e.g. less than 0.1ns for the SX-A device family). The HCLK network offers guaranteed low clock skew and clock propagation delay independent of the number of S-modules being driven. This enables excellent design performance and accurate pre-layout timing analysis.

Only one hardwired dedicated clock network exists on current antifuse parts.

Routed Clock Networks

Routed clock networks, specified by the names CLK, CLKA, CLKB, and Quadrant Clock (QCLK), are global clock networks that can be used both externally and internally (except for the CLK network in ACT1 family devices). The routed clock resources drive both sequential and combinatorial cells. This means they can be used as a fast track for non-clock signals, especially those with high fanout. The routed clocks are more flexible than the hardwired clock networks, but not as fast.

QCLKs, similar to CLKAs and CLKBs, can be sourced from external pins or from internal logic signals within the device. However, each of the individual QCLK resources can drive up to one chip quadrant, or they can be grouped together to drive multiple quadrants.

The number of available routed clock resources varies from device to device. See Table 1 on page 2 for details.

Special Clock Networks

In addition to hardwired and routed clock networks, there are other device-specific special resources in the ACT3 family. These resources cannot be driven by an internal logic signal.

IOPCL is a special hardwired input for I/O modules. It is wired directly to the Preset and Clear inputs of all I/O registers. IOPCL functions as an I/O when no I/O preset or clear macros are used.

IOCLK is a hardwired clock input for I/O modules (ACT3 device family). It is wired directly to each I/O register, and offers clock speeds independent of the number of I/O modules being driven. IOCLK can also be used as an I/O.

Table 1 summarizes the information on global clock networks—pad names, macro names, and the device families that support those networks. The table also indicates whether the clock network can be driven by an internal signal.

Clock Networks Architecture

Different clock networks have different architectures. A knowledge of clock network architectures will assist designers in utilizing these resources in the most efficient manner.

Hardwired Clock Network Architecture

HCLK is hardwired from the clock input buffer to the clock select MUX in each R-cell. Figure 1 shows the HCLK network architecture for SX-A family devices.

Table 1 • **Summary of Global Clock Network Resources**

Input Pad Name	Type	Family	Number	Internal Drive Option	Macro	Note
CLK	Routed	ACT1, 40MX, RT/RH1020	1	No	CLKBIBUF CLKBUF	
HCLK	Dedicated	ACT3, RT1400, RTSX, eX, RTSX-S, SX-A, SX	1	No	HCLKBUF	Connected only to sequential modulesf.
CLKA CLKB	Routed	ACT2, RT/RH, 1200XL, 3200DX, 42MX, SX, SX-A, eX, RTSX-S,	2	Yes	CLKBIBUF CLKBUF CLKINT	Use CLKINT for internal drive option. Does not include RH/RT 1020 devices.
IOCLK	Dedicated	ACT3, RT1400	1	No	IOCLKBUF	Connected to all I/O modules.
IOPCL	Special	ACT3, RT1400	1	No	IOPCLBUF	Connected to I/O module Set and Reset pins.
QCLK	Routed	3200DX, 42MX, SX-A, RTSX-S	4	Yes	QCLKBUF QCLKINT QCLKBIBUF	Use QCLKINT for internal drive option. QCLKBIBUF only applies to RTSX72S and A54SX72A devices.

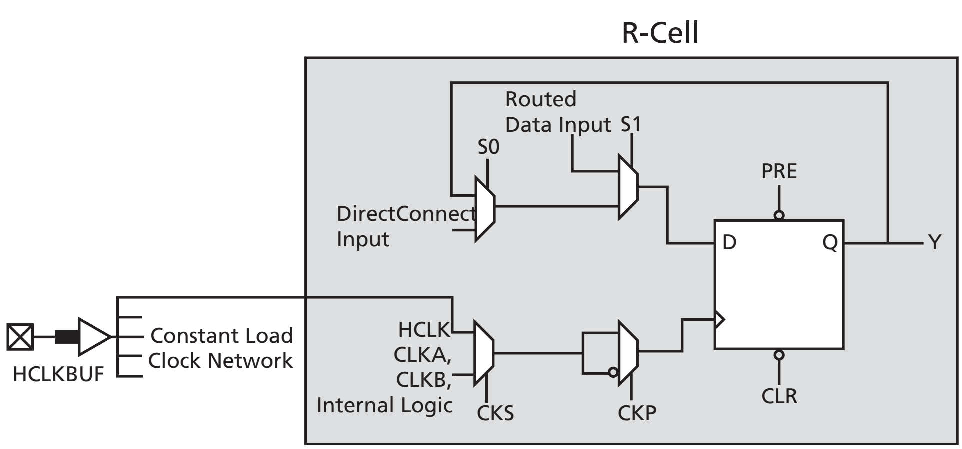

Figure 1 • **HCLK Network for an SX-A FPGA Family**

Due to elimination of programming elements (fuses) from the path, the HCLK network is the clocking resource with the lowest skew.

As shown in Figure 1 on page 2, the inputs of the dedicated clock networks are hardwired to the pads. In other words, these resources cannot be driven by internal signals. Users should keep in mind that the hardwired clock network is connected only to the clock input of sequential macros, so it cannot be used to drive combinational cells. As a result, CC macros cannot be driven by the hardwired clock network.

In device families with I/O registers (such as ACT3), a dedicated clock network is provided to drive the clock input of those registers with a guaranteed speed (IOCLKBUF). Note that these dedicated clock signals cannot be connected anywhere else.

RTSX-S, SX-A, and eX families have the same circuit. Family devices contain an HCLK Reset Synchronizer circuit. The logical implementation of this HCLK Reset Synchronizer can be seen in Figure 2. When the device is powered up but the internal device charge pump has not yet been turned on, the four flip-flops in the circuit are reset to '0'. Since the four flip-flops are configured in a shift register configuration with the first flip-flop data input in the shift register biased to '1' (V_{CCA}), it takes four CLK cycles to get all four flip-flops back to the '1' (enable) state. On the fourth clock pulse, the fourth flip-flop sets, and that clock pulse propagates into the logic array. Additionally, the TRST signal is logically AND-gated with the internal JTAG power-on reset signal, and its output drives the preset input of the four flip-flops. The preset input on the four flip-flops has precedence over the clear input. Therefore, if the TRST signal is asserted by biasing the external pin to ground, the four flip-flops are all forced to '1', which allows the initial four HCLK pulses to pass to the array logic. However, if the clock is a free-running signal, the HCLK Reset Synchronizer circuit should not matter in the board-level design.

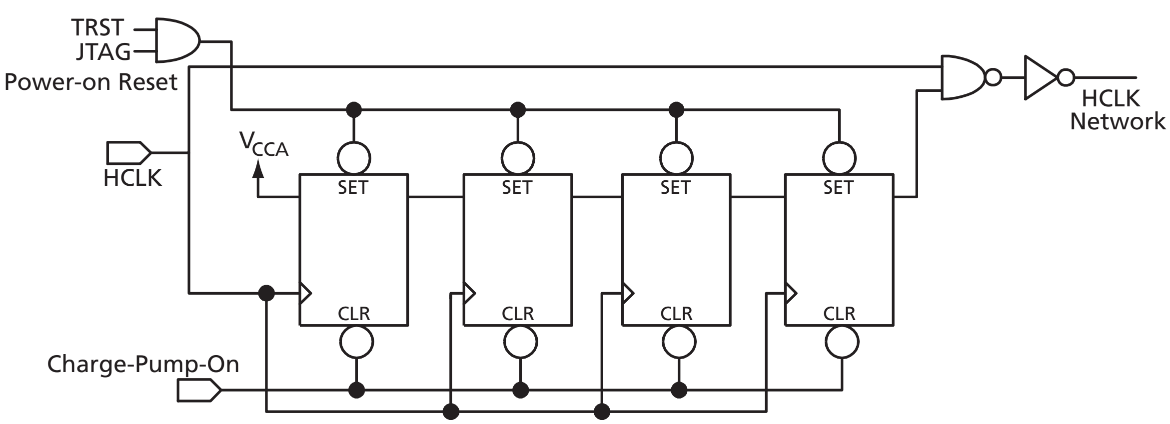

Figure 2 • **HCLK Reset Synchronization in SX-A, eX, and RTSX-S Devices**

Routed Clock Network Architecture

Routed clock networks can be driven by either external or internal signals via a MUX architecture. The CLKA and CLKB routed networks are identical. Signals are buffered prior to entering the clock network. Figure 3 on page 4 illustrates the architecture of these routed networks for the SX-A FPGA family (except A54SX72A—see Figure 4 on page 4).

As shown in Figure 3 on page 4, the registers for the clock network can be clocked by either the positive or negative edge of the clock signal. If CLKA/B is not used externally, these clock pins must be set to logic LOW or HIGH on the board. They should not be left floating.

Routed clock networks can be driven by either external or internal signals, and drive both sequential and combinational cells. This means they can be used as the clock network to drive CC macros, especially in radiation-hardened and radiation-tolerant devices.

The quadrant clock architecture is similar to the CLKA/B, except that it provides a low-skew network in a single-chip quadrant. This allows designers to use different quadrants of the low-skew network for different signals or clocks. This feature is especially valuable for designs in which there are several signals with strict timing skew requirements or multiple blocks driven by separate clock signals.

If the QCLK pins are not used, they can be configured as user I/Os. Figure 4 shows the architecture of the QCLK network in the A54SX72A device. The A54SX72A and RT54SX72S CLKA/CLKB networks contain an additional feature—the internal logic is buffered so it can drive both an external pad and the QCLK network.

Legacy device families (ACT1 prior to 1010B and 1020B) exploit row-buffered routes to establish a high-fanout clocking network. Figure 5 on page 5 illustrates the row-buffered clock network architecture for the 1010A FPGA family. In this architecture, clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

Designs in device families with the global clock network architecture, as shown in Figure 5 on page 5, require more attention to place and route. The global clock network in the old FPGA families has considerable path delay and clock skew compared to the newer device families. Therefore, if the routing path lengths from the clock input pin to different registers are very different, there will be a considerable clock skew for those registers. To avoid this undesirable clock skew, Actel recommends that the registers driven by the same clock be placed as close together as possible to prevent unnecessarily long paths for the clock signal. Actel's place-and-route tool will do this automatically. In addition, the Designer software's ChipEditor tool provides a manual placement option if replacement of a few registers might improve the design’s timing characteristics. One way to influence place and route is to impose timing constraints on the place-and-route tool via SDC format constraints such as set_max_dely, which limits delays between registers (refer to the *Using Synopsys Design Constraints (SDC) with Designer* application note).

In the B die version of ACT1 family and similar devices (i.e. 40MX and RH), the clock network uses an independent TTL driver to increase the clock network’s speed and drive. In addition, the row drivers are shorted together, which allows a lightly-loaded row to offer charging current to a heavily-loaded neighboring row. The result is a markedly reduced clock skew between rows.

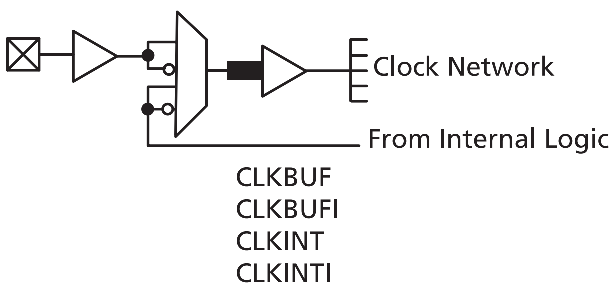

Figure 3 • **SX-A Routed Clock Architecture**

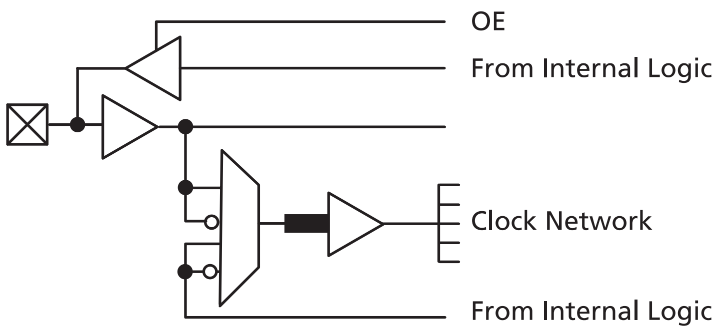

Figure 4 • **A54SX72A Routed Clock Structure**

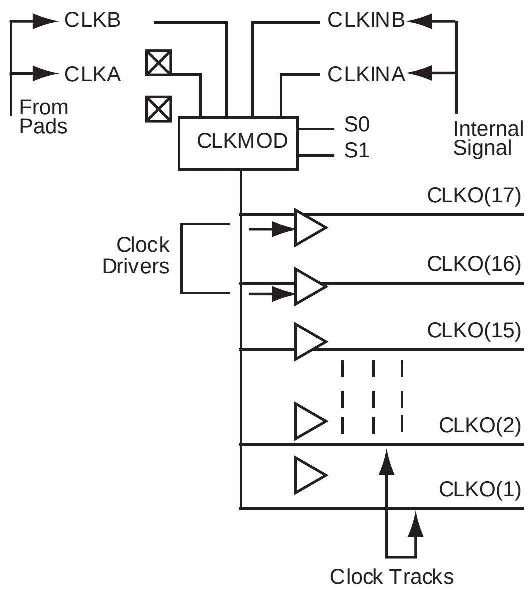

Figure 5 • **Clock Networks**

Clock Network Assignment

Hardwired clock networks and CLK in the ACT1 FPGA family can only be driven by external input signals. Other clock resources can be connected to either external or internal signals. Clock networks are assigned to different signals by instantiating the correct macros. Actel's Designer software recognizes the macro and, based on its type, assigns the proper clock network to the signal driving that macro.

If designers do not specify global clock network assignments, synthesis tools will assign clock networks based on the synthesis tools' predetermined priorities. These priorities are mostly set by the fanout of each signal. Synthesis tools attempt to assign low-skew resources to signals with high fanout (e.g., global reset, enable, or clock signals). QCLK networks are not instantiated automatically by synthesis tools. As a result, CLKA and CLKB global resources are the synthesis tools' first targets for assignment to high-fanout nonclock signals. To improve performance, designers can take control of the clock network assignment by instantiating proper macros or attributes in the design. The following sections of this document discuss these techniques.

Dedicated Clock Assignment

There are three dedicated clock networks: HCLK, IOCLK, and IOPCL.[1] Assignment of these clock networks to external signals is accomplished by instantiating HCLKBUF and IOCLKBUF macros. Figure 6 on page 6 shows these macros.

Based on the design flow environment, there are different ways to instantiate these macros. In a schematic design, the user should simply import the macro from the Actel cell library into his/her design with its PAD and Y ports connected to the input clock signal and clock network, respectively. In HDL flow designs, users can instantiate the macro in their code. Table 2 on page 6 describes the basic coding style for instantiation of HCLKBUF. If not instantiated manually, the HCLK network will be assigned at the discretion of the synthesis tool to the clock signals, driving only sequential cells with the highest fanout or most critical timing.

Designers must avoid conflicts between pin configurations and HCLK network assignment of the input signals. Keep in mind that the HCLK network is hardwired to a specific pin number in each device, and the signal that drives this network must be assigned to that specific pin.

1. *IOCLK and IOPCL can only be found in ACT3 devices.*

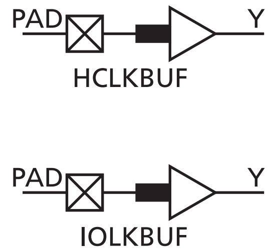

Figure 6 • **Dedicated Hard-Wired and I/O Clock Buffers**

Table 2 • **HDL Instantiation of HCLKBUF**

HDL instantiation of HCLKBUF	
VHDL	**Verilog**
library IEEE;	module design (……………);
use IEEE.std_logic_1164.**all**;	input …………………;
entity design **is**	output …………………;
port (………………… : **in** std_logic; ………………… : out std_logic); end design;	HCLKBUF U2 (.Y(clk_net), . .PAD(input_clock)); ……………………
architecture rtl **of** design **is**	……………………
-- Component Declaration **component** HCLKBUF	**endmodule**
port (PAD : in std_logic;	
Y :out std_logic);	
end component; begin -- Concurrent Statement	
U2 : HCLKBUF **port map** (PAD => input_clock,	
Y => clk_net);	

Routed Clock Assignment

Different routed clock macros have been provided for different purposes. They can be categorized as either I/O clock buffers or internal clock buffers. I/O clock buffers are used to route external clocks to the clock networks, while internal clock buffers assign internal signals to the routed clock network. Figure 7 illustrates these buffers for the CLKA or CLKB routed clock. (For the QCLK network, QCLKBUF and QCLKINT are similar to CLKBUF and CLKINT respectively).

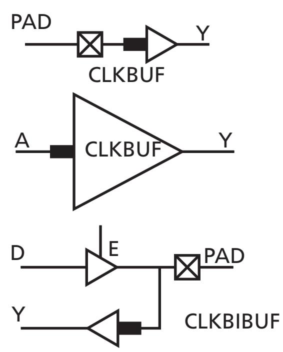

Figure 7 • **Routed Clock Buffers**

The instantiation of CLKBUF and QCLKBUF is very similar to HCLKBUF, explained in the previous section. The following section discusses the coding styles that achieve the highest network flexibility.

Assigning Internal Logic to the Routed Clock Network

To reduce delays and timing skew, internal signals with high fanout can be assigned to routed clock networks. CLKINT or QCLKINT should be instantiated in the design. This is similar to the use of CLKBUF, except the input port name "A" replaces "PAD" for (Q)CLKINT. The outputs of these macros will be connected to the routed clock network.

In some cases, the clock signal is generated internally as a part of the FPGA design, while other sections of the FPGA use the generated clock. Actel recommends connecting the clocks to the global networks internally via instantiation of CLKINT or QCLKINT, rather than exporting them from the chip to the board and importing them back into the FPGA through another input pin.

Assigning a Regular I/O Pin to the Global Clock Network

In some cases, the designer needs to drive the clock network with non-clock input pins. This may be due to board limitations where the designated clock input pins cannot be used. In this case, the clock signal must be sourced by a regular input buffer (such as INBUF), then connected to a global clock resource. This can be accomplished by simply connecting the output of the INBUF to the input of (Q)CLKINT.

Preserving Global Clock Networks

Synthesis tools usually assign clock buffers to clock signals. In situations where clock resources are limited, the designer can control the usage of global clock resources by specifying the clocks that do not need a clock buffer. This can be done by instantiating regular I/O buffers in a schematic design for the clock signals, or by adding attributes to the HDL code. Different synthesis tools use different attributes. Table 3 on page 8 describes the attribute in both VHDL and Verilog for Synplicity.

Table 3 • **Syn_noclockbuf Attribute of Synplicity**

Attribute: Syn_noclockbuf
VHDL: (CLK is the name of the clock signal) attribute syn_noclockbuf : Boolean; attribute syn_noclockbuf of CLK : signal is true;
Verilog: Module example (CLK); input CLK /* synthesis syn_noclockbuf =1 */; …………… endmodule

In the Synopsys synthesis tool, the dont_use and dont_touch attributes have the same functionality.

Other Design Considerations

Many designers have concerns about global clock networks regarding the capability of driving I/O macros, reset or preset of registers, and flip-flop data input. As mentioned earlier, I/O macros can be driven only by dedicated networks.

Routed clock networks can be connected to registers' reset or data inputs. The user should take care when driving data inputs of registers. If the routed clock network is connected to a sequential cell's register data input, a buffer is needed in the data path. These buffers change the signal name and bring the data out of the clock network. In such cases the Designer software inserts a buffer (BUFF) automatically, and issues a warning to notify the user.

In a situation where the routed clock also drives combinational cells, buffer insertion might be needed. The architecture of Actel's antifuse FPGA combinatorial cells is based on MUX blocks. If the routed clock network is connected to the signals feeding the MUX blocks data input (D0 through D4 in eX C-cell architecture), BUFF insertion is not needed. However, if the routed clock network drives the signals connected to the MUX blocks selection lines (A0 and B0 in eX C-cell architecture), the Designer software will insert a BUFF. The place-and-route tool issues a warning message when it carries out the automatic BUFF insertion.

In some cases, especially in designs that contain a large number of clock networks, it is necessary to implement the networks using balanced buffer trees made up of local routing resources. It is important to equalize the fanout for different branches of the clock tree to reduce clock skew between branches. This can be done by using Actel Silicon Expert software, included on the Designer CD. The software automatically balances the fanout of each branch, thus reducing clock skew.

There is one important factor in assigning signals to QCLK global networks. Since each QCLK network spans only a quadrant of the chip, a single macro cannot be driven by more than one QCLK network unless the networks are tied to each other. Designer automatically ties quadrants together if the fanout for an assigned clock is greater than one quadrant.

The Designer software also automatically assigns the quadrant in which the clock network will reside. In some cases, the user wants the signal to be in a specific quadrant of the chip. The first of three possible approaches to performing user-specified QCLK assignment is:

- If the driving signal is connected to an external input, the user can simply assign the signal to the desired QCLK input pin (via PinEditor or Pin file). By doing this, the place-and-route tool is forced to assign the specified quadrant network to the desired input.

The other two approaches should be taken after a preliminary layout, and are especially useful when the driving signal is internal. Both require the use of the Designer software's ChipEditor tool:

- Another approach is to select, drag, and drop one of the macros in the used QCLK network into the unused desired quadrant network. Then, the user needs to fix this placement while still in ChipEditor mode, commit the changes, and do the place and route again. Since the new placement of that specific macro is fixed, the placer is forced to assign all other related (eventually the whole quadrant) macros to the new quadrant of the chip.
- The last approach is to simply drag and drop the used quadrant macro into the unused, desired one. This can be done in ChipEditor mode.

Note that the new placement should be fixed and committed before exiting ChipEditor mode. Figure 8 on page 9 indicates two of the quadrant network macros.

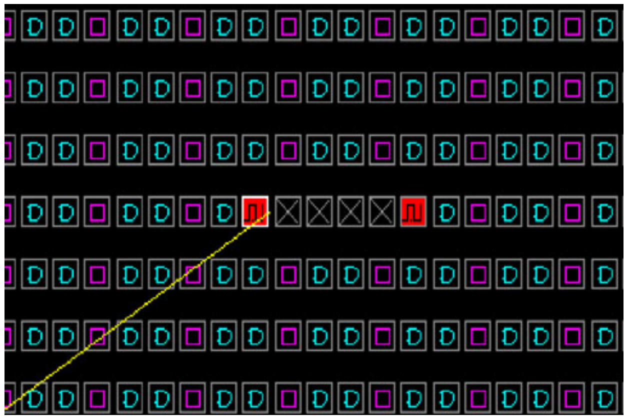

Figure 8 • **Quadrant Network Macros**

I/O Thresholds

In eX, SX-A and RT54SX-S devices, the I/O standard of the clock buffers (HCLKBUF, CLKBUF and QCLKBUF) are controlled by a global fuse. This means that assigning an I/O standard to one of those buffers will define the standard for all other input clock buffers. Furthermore, the input clock buffers (HCLKBUF and Q/CLKBUF) of SX-A and RT54SX-S devices do not contain a PCI clamp diode. In other words, when set to the PCI standard, the input clock buffers comply with the PCI standard threshold voltage requirement, but do not have the clamp diode. Figure 9 on page 10 shows the input clock buffers for RT54SX32S device.

As mentioned earlier in the "Routed Clock Network Architecture" on page 3, the architecture of the routed clock inputs is slightly different in the A54SX72A and RT54SX72S devices. As shown in Figure 10 on page 10, these devices' routed clock inputs can also be employed as user I/Os because they contain a regular I/O buffer structure in their architecture. The following list describes the advantages of this additional I/O buffer in the routed clock input architecture that enable more flexibility:

- PCI clamp diode: If the users have set the I/O standard of the routed clock inputs to PCI and need the clamp diode on this input, they can utilize the routed clock inputs as a regular user I/O by using INBUF instead of Q/CLKBUF. The output of the INBUF can be connected immediately to a Q/CLKINT to drive the global routed clock networks. In this case, the regular I/O architecture (which includes a clamp diode) will be used in the routed clock network input.
- CMOS standard: As it has been presented in Figure 9 and Figure 10 on page 10, the global clock buffers of eX, SX-A and RT54SX-S devices do not support the CMOS input standard. A54SX72A and RT54SX72S devices enable designers to connect a CMOS standard clock signal to the routed clock network. Since the regular I/O buffers (INBUF) support the CMOS standard, the designer can connect the clock to the routed clock input pin using a regular INBUF (embedded in the routed clock input architecture), set the I/O standard to CMOS, and use a CLKINT immediately after the user I/O to drive the global routed clock network.

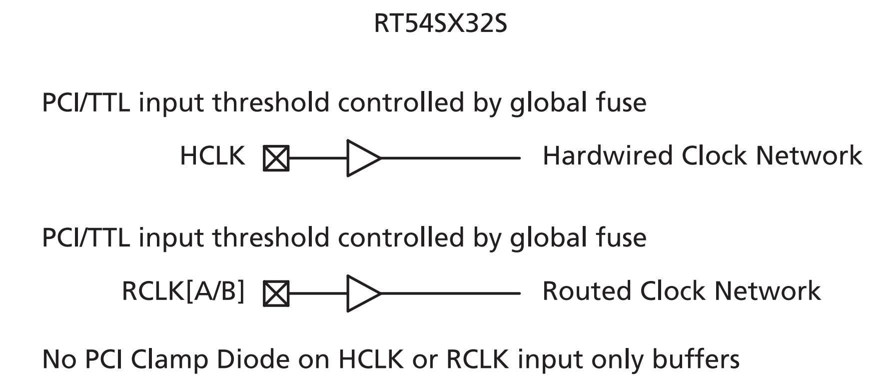

Figure 9 • **Input Clock Buffers in RT54SX32S Devices**

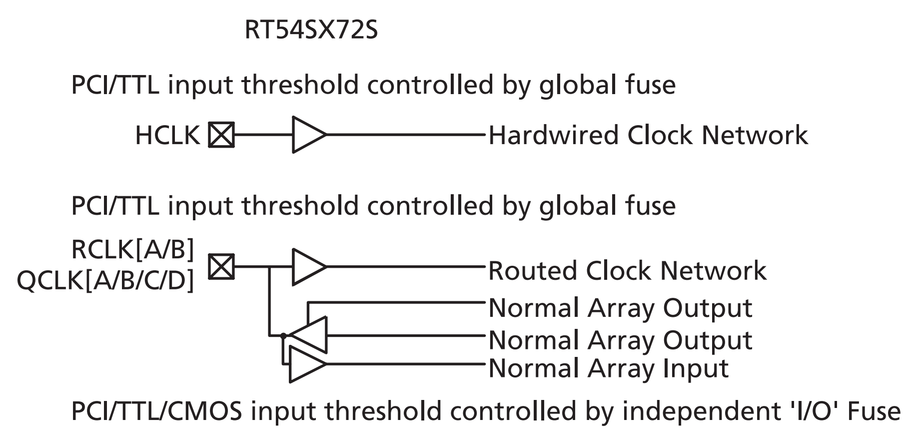

Figure 10 • **Input Clock Buffers in RT54SX72S Devices**

Board-Level Considerations

The shape of the clock signal's input to the FPGA is very important for proper device functionality. One important characteristic of an input clock signal is its slew rate. Actel's antifuse FPGAs have different slew-rate requirements for their clock input. The clock slew-rate requirements can be found in the device datasheet. If the clock signal's slew rate is slower than that required for the device, the clock signal's logic after the input buffer will be unknown, resulting in improper functionality.

Another important parameter that affects the external clock signal shape is distortion. For example, improper line termination of the clock path can result in uncontrolled reflections (similar to wave reflection in a wave guide). These uncontrolled reflections on termination points might result in unwanted spikes on the clock. For example, these spikes might be taken by FPGA logic as active clock edges, which will result in mis-functionality of the design. If the clock line is not properly terminated, Actel recommends AC termination of the clock line. This involves placing a resistor and capacitor pulled down to ground at the clock input of the device, as shown in Figure 11. This RC filter will stop the unwanted spikes from propagating into the FGPA.

The R and C values follow these general rules:

R should be equal to Z0, where Z0 is the impedance of the clock line. By selecting the proper value for R, the reflection coefficient of the line will cancel out any reflected signals. In other words, the reflections of the clock signal will be absorbed at termination.

The C value should be chosen so that it makes the RC time constant approximately 1/3 of the clock period. This will make the clock edges fast enough, and acceptably noise-free.

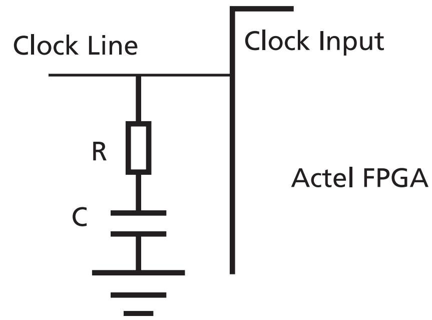

Figure 11 • **AC Termination at the Clock Input**

Conclusion

Actel devices provide different clock network resources for various applications. Utilizing the appropriate network enables users to achieve very high performance without going through extensive logic-level reduction in their designs. Actel global clock networks provide different levels of flexibility to fit into various applications without sacrificing design efficiency.

Related Documents

Application Notes

Using Synopsys Design Constraints (SDC) with Designer

http://www.actel.com/documents/SDC_AN.pdf

List of Changes

Previous Version	Changes in Current Version 5192695-3/06.04*	Page
5192695-2/02.03	Table 1 was updated.	2
	The "Hardwired Clock Network Architecture" section was updated.	2

Note: * The part number is located on the last page of the document.

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