

Prototyping With AFS600 for Smaller Devices

This document is designed as an aid for customers who may ultimately wish to use one of the smaller members of the Fusion family (AFS090 and/or AFS250). The first device available in the Fusion family is the AFS600, which can be used as a development or prototyping platform for the smaller devices. This document will help highlight differences between the AFS600 and these smaller devices in order to ease transition to the targeted device when it becomes available.

The Fusion family, based on the highly successful ProASIC[®]3E and ProASIC3 Flash FPGA architecture, has been designed as a high-performance, programmable, mixed signal platform. By combining an advanced flash FPGA core with embedded flash memory and analog peripherals, Fusion devices dramatically simplify system design, and save overall system cost and board space as a result. [Figure 1](#) shows the Fusion device architecture overview.

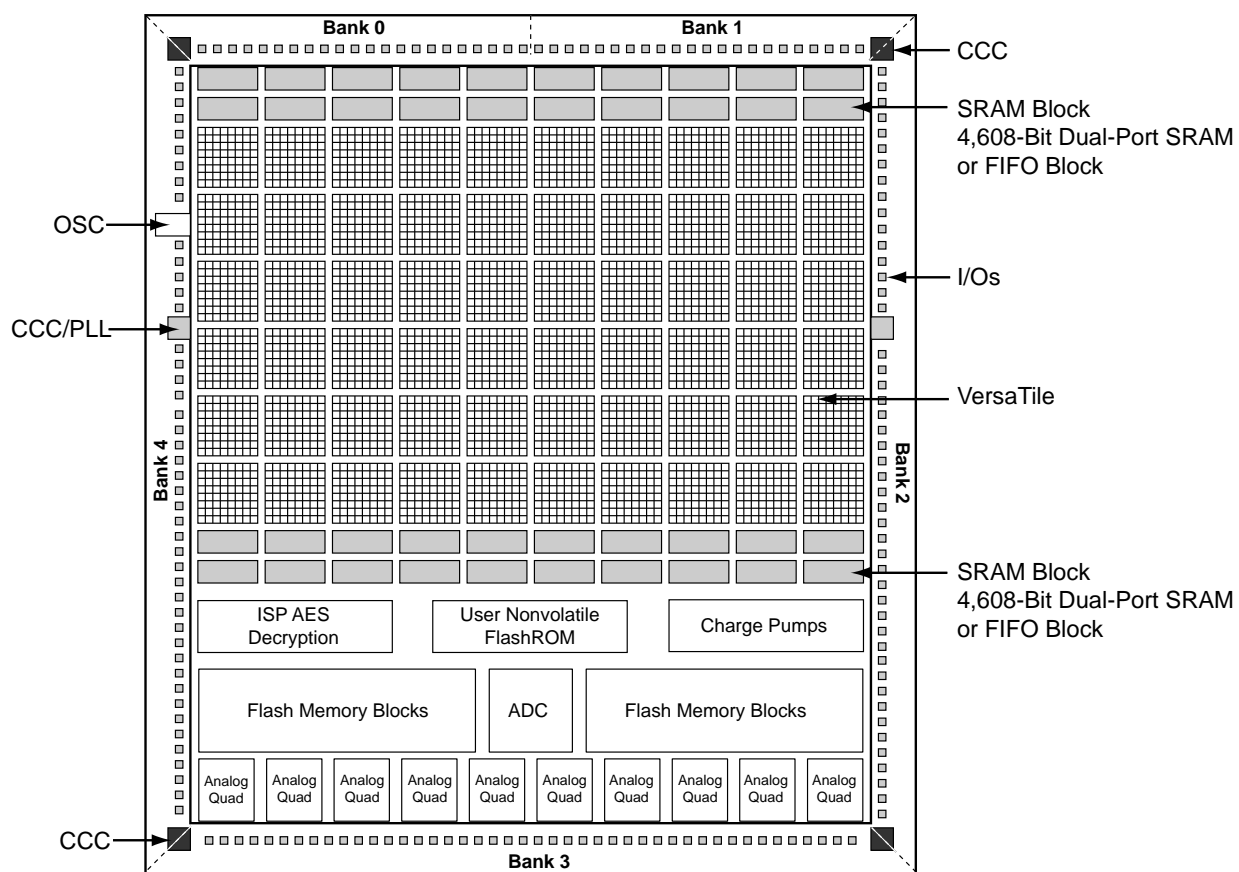


Figure 1 • Fusion Device Architecture Overview

The state-of-the-art embedded flash memory technology offers high-density integrated flash memory arrays, enabling savings in cost, power, and board area relative to external flash solutions, while providing increased flexibility and performance.

Fusion devices offer a robust and flexible analog mixed signal addition to the high-performance flash FPGA fabric and embedded flash memory. The many built-in analog peripherals include a configurable 32:1 input analog multiplexer, up to 10 independent metal-oxide semiconductor field-effect transistor (MOSFET) gate driver outputs, and a configurable analog-to-digital converter (ADC). The Analog Quad is an I/O structure that contains three adjacent analog inputs and a gate driver output.

The addition of the real-time counter (RTC) system enables Fusion devices to support both standby and sleep modes of operation, greatly reducing power consumption in many applications.

Prototype Guideline

AFS090, AFS250, AFS600, and AFS1500 Device Configuration

AFS600 is a medium size device in the Fusion family. It supports all of the Fusion features, as shown in [Table 1](#). The smaller devices (AFS090 and AFS250) in the Fusion family have lower gate counts and fewer memory blocks, I/Os, and PLLs.

Table 1 • AFS090, AFS250, and AFS600 Device Summary

Part Number		AFS090	AFS250	AFS600	AFS1500
General Information	System Gates	90,000	250,000	600,000	1,500,000
	Tiles (D-Flip-Flop)	2,304	6,144	13,824	38,400
	Secure (AES) ISP	Yes	Yes	Yes	Yes
	PLLs	1	1	2	2
	Globals	18	18	18	18
Memory	Flash Memory Blocks (256 kbytes)	1	1	2	4
	Flash Memory (kbytes)	256	256	512	1,024
	FlashROM Bits	1 k	1 k	1 k	1 k
	RAM Blocks (4,608 bits)	6	8	24	60
	RAM kbits	27	36	108	270
Analog	Analog Quads	5	6	10	10
	Analog Input Channels	15	18	30	30
	Gate Driver Outputs	5	6	10	10
I/O	I/O Types	Analog/ LVDS/Std+	Analog/ LVDS/Std+	Analog/ LVDS/Pro	Analog/ LVDS/Pro
	I/O Banks (+ JTAG)	4	4	5	5
	Maximum Digital I/Os	73	114	172	278
	Analog I/Os	20	24	40	40
I/O: Digital/Analog	QN108	36/14		–	–
	QN180	48/20	62/24	–	–
	PQ208	–	93/24	95/40	–
	FG256	73/20	114/24	119/40	119/40
	FG484	–	–	172/40	228/40
	FG676	–	–	–	278/40

Table 2 shows compatible devices for each package. The FG256 package is designed to support migration across all family members.

Table 2 • Package Compatibility Table

Package Types	PQ208	PQ208	FG256	FG484	FG676	QN108	QN180
Compatible Devices	AFS90	AFS600	AFS090	AFS600	AFS1500	AFS90	AFS090
	AFS250	AFS1500	AFS250	AFS1500			AFS250
			AFS600				
			AFS1500				

List of the Guidelines for Prototyping

Microsemi recommends AFS600-FG256 as the platform for prototyping smaller devices within the same compatible package type. AFS600-FG256 is also the first available Fusion silicon in the rollout roadmap and is used in the Fusion Starter Kit, which can serve as a prototype board to demonstrate the majority of Fusion features.

Memory Blocks

The AFS250 and AFS090 have a single 256-kbyte block of embedded flash memory, whereas the AFS600 has two 256-kbyte blocks (512 kbytes total). Therefore, the user must keep the usage less than 256 kbytes while doing prototyping with the AFS600.

The AFS250 has 8 RAM blocks, while the AFS600 has 24 RAM blocks. A SmartGen analog system generated soft IP uses 3 to 9 blocks of RAM. The user needs to keep track of the RAM block usage, especially if the design contains a RAM initialization application, data storage application or other applications that utilize extra RAM blocks. Usage must be no more than 8 blocks. Likewise, if the user is prototyping for AFS090, then the RAM block usage in AFS600 should not exceed 6 blocks.

PLLs

The AFS250 and AFS090 have one PLL on the west side of the device, whereas AFS600 has two PLLs—one for each side of the device. During prototyping using AFS600, the user should only implement the PLL on the west side and use the corresponding PLL input pin, so that the delays from the PLL input through the PLL to the global network have a minimum variation between AFS090/AFS250 and AFS600.

I/Os

All special function I/Os (V_{CC} , GND, JTAG, Programming Control, etc.) of the AFS250 and AFS090 devices are in exactly the same locations as in the AFS600 device, with one exception for the AFS090 as listed below. The AFS250 device has 6 Analog Quads, whereas the AFS600 device has 10 Analog Quads. The user should only use Analog Quads 0–5 while doing prototyping in AFS600, in order to have exactly the same analog pin map. To prototype AFS090, the user should only use Analog Quads 0–4, since AFS090 has 5 Analog Quads.

While the AFS250 differential I/Os have the same locations as the AFS600, the AFS090 differential I/O locations are slightly different from those of the AFS600. More details on the pin list are available in the *Fusion Family of Mixed Signal FPGAs* datasheet. The user should be aware that if the design has differential I/Os, the pinout needs to be changed from the AFS600 prototype design to an AFS090 production design.

Prototype Consideration in Software

After validating the design in the AFS600, the user needs to create a new Libero[®] System-on-Chip (SoC) software project for the AFS090 or AFS250, then recreate the SmartGen cores by using the same parameters used for the AFS600. All other source code used in the AFS600 project can be directly imported into the AFS090 or AFS250 project. The same validation process (simulation, static timing analysis, and functional test on silicon) should be performed for the AFS090 or AFS250 design as the user has done for AFS600.

Summary

AFS600-FG256 is the recommended Fusion prototyping vehicle for smaller devices in the same compatible package. It is also used on the Fusion Starter Kit board, which can demonstrate most of the Fusion family features.



Microsemi[®]

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at www.microsemi.com.

© 2011 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.