

Temperature, Voltage, and Current Calibration in Fusion FPGAs

Introduction

Actel Fusion[®] mixed signal FPGAs integrate configurable analog features, including I/Os, prescalers, low-pass filters, and an analog-to-digital converter (ADC), enabling customers to perform temperature, voltage, and current measurements in their applications. Analog components have a specific accuracy for a given set of conditions. The accuracy can have a broad range of definitions and is affected by many parameters in the system. For example, in a temperature measurement application, the accuracy of the measured temperature is influenced by the accuracy of on-chip elements (temperature sensor, op amps, and ADC), use model (sample rate, ADC resolution setting, post-processing, etc.), and board-level considerations. For the purpose of this document, accuracy can be defined as the difference/error between the actual value and the measured value. For example, in a temperature measurement application, an accuracy of $\pm 2^{\circ}\text{C}$ means that the measured value may be up to $\pm 2^{\circ}\text{C}$ different from the actual value.

If the difference between the measured value and the actual value is too great, you can use calibration to bring the measured value closer to the actual value. Calibration assumes a profile for the relationship between the actual value and the measured value. This profile depends on the characteristics of the components used in the measurement. There are two calibration profiles: one corrects for offset error only, and the second accounts for both offset and gain errors. [Figure 1](#) illustrates these typical profiles that define the calibration implementation methodology.

To completely calibrate a system, users can calibrate individual components, or they can calibrate the entire system, taking into account the error of all the individual components working together. Many users may decide to perform both levels of calibration. This document provides a description of the factory calibration methodology for voltage inputs on Fusion devices, and also provides recommendations on system calibration methods for voltage, temperature, and current using Fusion. Using Actel's device calibration solution, the Fusion ADC sampling accuracy for voltage prescaler inputs can be improved to 1%, enabling Fusion to better meet customers' design requirements.

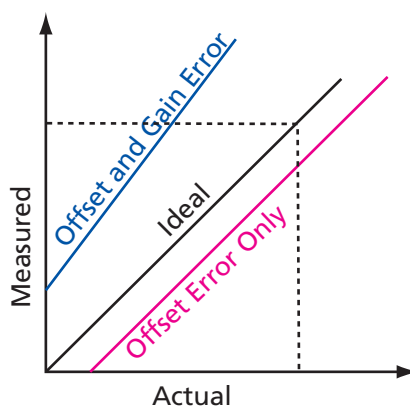


Figure 1 • Example Profiles of Measured Value and Actual Value Variations

General Calibration Concept

Calibration Methods

Based on the measured-versus-actual profile and the required accuracy, customers can define the most efficient method for translating the measured value into an actual value. In most analog components, including the Fusion FPGA, the relationship between measured and actual values follows the profiles illustrated in [Figure 1 on page 1](#). This document describes only calibration methodologies associated with offset-only and offset-and-gain corrections.

Offset-Only Calibration

Offset-only calibration (sometimes known as one-point calibration) is based on the relationship between the measured and actual values given in [EQ 1](#):

$$y = x + c$$

EQ 1

where

- y = actual value
- x = measured value
- c = offset compensation between measured and actual values

As shown by [EQ 1](#), offset-only calibration accounts for the offset between the actual and measured values.

Offset-and-Gain Calibration

If the correlation between the actual and measured values is defined primarily by an offset, as shown in the offset error line in [Figure 1 on page 1](#), or if the actual measured value is naturally constrained to a specific region, offset-only calibration may be sufficient to achieve a high degree of accuracy.

However, in some cases, especially if the range of the measurement varies widely, the difference between the actual and measured values not only includes an offset but is also governed by a gain variation, as shown in [Figure 1 on page 1](#). In such cases, offset-only calibration may not provide sufficient correction to achieve the accuracy required by the customer's application. In this case, offset-and-gain calibration (also known as two-point calibration) can be implemented to achieve a higher level of accuracy.

In two-point calibration, the relationship between the measured and actual values is governed by [EQ 2](#):

$$y = mx + c$$

EQ 2

where

- y = actual value
- x = measured value
- c = offset compensation between measured and actual values
- m = gain compensation between measured and actual values

Choosing between one-point calibration and two-point calibration depends on many parameters, some of which include the following:

- Customer application's required accuracy
- Measurement gain and offset error of electrical components, such as the Fusion FPGA
- Application's operating range

Customer Application's Required Accuracy

Given the required accuracy of an application within its operating range, designers can use the specified gain and offset error of Fusion FPGAs to determine the suitable calibration method to achieve the desired accuracy. Refer to the *Fusion Family of Mixed-Signal Flash FPGAs* datasheet for more information.

Calibration Measurements

To calculate m or c in EQ 1 and EQ 2 on page 2, measurements must be taken in a known environment so measured data can be compared against actual values. The number of required data points depends on the method of calibration. One data point would suffice for one-point calibration (determining offset), whereas for two-point calibration, two data points are needed to define gain and offset. In calibration measurements, a known actual value (temperature, current, or voltage) is supplied to the system, and the measured value is recorded.

Offset-Only Calibration Measurement

In offset-only (or one-point) calibration measurement, an actual value of P_{a1} (e.g., temperature) is applied to the system, and its value is measured as P_{m1} by the system. Then, the offset value c in Figure 1 on page 2 can be calculated as shown in EQ 3.

$$c = y_1 - x_1$$

EQ 3

Offset-and-Gain (two-point) Calibration Measurement

As shown in Figure 2, to calculate m and c in EQ 2 on page 2, two data points are needed for two-point calibration.

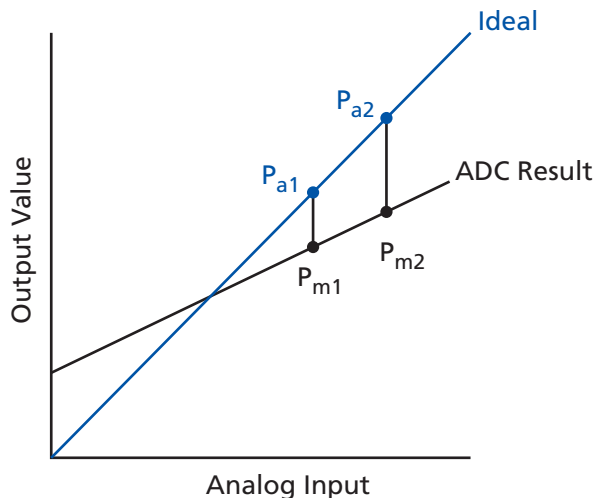


Figure 2 • Two-Point Calibration for Offset-and-Gain Error

Therefore, two known actual values (y_1 and y_2) must be applied to the system, and two measured points (x_1 and x_2) must be recorded. The m and c values in EQ 2 on page 2 are calculated as shown in EQ 4 and EQ 5.

$$m = (y_2 - y_1) / (x_2 - x_1) \tag{EQ 4}$$

$$c = (y_1 \times x_2 - y_2 \times x_1) / (x_2 - x_1) \tag{EQ 5}$$

Choosing Calibration Data Points

In one-point calibration, from a practical point of view, Actel recommends that the applied actual value be in the middle of the operating range as defined by the application. For example, if the system measures a voltage that operates from 0 V to 5 V, taking the calibration measurement at ~2.5 V will typically give the best results.

For two-point calibration measurement, Actel recommends that the two data points be taken at 20% and 80% of the operation range. For example, if a temperature measurement application is used in a system that operates from 0°C to 50°C, Actel recommends that the calibration measurements be taken at 10°C and 40°C.

In many voltage or current monitoring applications where the operating range includes 0 V or 0 A, customers tend to choose 0 V or 0 A as one of their calibration measurement data points. This is mainly driven by the simplicity of setup for measurements at the ground level. However, the ground level of the system is typically noisy due to the operation of the system and other noise factors. In such situations, the calibration measurement may not be sufficient to achieve the accuracy level required by the overall design. Therefore, Actel recommends that zero-level measurements be avoided for voltage and current calibration data collection.

Actel Fusion FPGAs offer up to 32 analog channels for temperature, current, or voltage measurements. Many applications, such as system management, use more than one analog channel in their design. Though all these channels use a single ADC inside Fusion, each prescaler circuit within the analog I/O structure has a unique set of op amp circuits. Therefore, it is necessary to calibrate each channel that requires the increased level of accuracy independently. In this case, each channel has its own calibration coefficient based on the method used for calibration (one-point or two-point).

Furthermore, in an analog (voltage/current/temperature) measurement, application designers exploit other components besides the Fusion FPGA to sense, transport, or amplify the measured parameters.

Customers can use two general approaches in calibrating these systems:

1. Calibrate each device used in the measurement individually.
2. Calibrate all the utilized devices when operating together in the system.

In the first approach, the customer calibrates each device individually in a controlled setting. In this case, the methods and recommendations explained in this document are applicable for the Fusion device. For other components, the customer should follow the recommendations and techniques provided by the vendor of each component.

In the second approach, all the system components in the application are used to take the calibration data points. In this case, the total measurement error can be adjusted by calibrating the measured values after the ADC. If this method is used, all the recommendations and techniques in this document can be applied.

Actel Calibration Solution

Actel's device-level calibration solution offers significant improvement in ADC accuracy for voltage monitor applications. There are two ways of exercising the Fusion ADC for voltage monitoring: sampling prescaled analog input or sampling direct analog input. If a customer design requires better accuracy than the default Fusion ADC performance, then calibration is needed. Since direct analog input sampling accuracy is well within 1%, the Actel calibration solution does not offer any additional benefit, so it is only available for prescaled inputs.

Temperature and current monitor calibration are not supported.

The Actel calibration solution is a two-point offset-and-gain calibration scheme. The implementation is performed through the following two steps:

1. During production test and screening flows, m and c compensation values are determined for each analog voltage channel and stored in the flash memory block of each Fusion device.
2. In Actel Libero® Integrated Design Environment (IDE) v8.2 SP1 and later, an RTL calibration IP block is built into the SmartGen Fusion Analog System Builder core. This calibration block reads the m and c values stored in the flash memory and uses them to calibrate data for each analog voltage channel.

Coefficient Measurement and Programming

During the Fusion production test flow, in a controlled environment, Actel measures the calibration coefficients, m and c , of every prescaler level of all 30 channels of each device. Measurements are done with the Fusion ADC VAREF set to 2.56 V. In other words, the coefficients do not apply to any customer designs that use a VAREF other than 2.56 V. Actel calibration implementation is disabled in software when VAREF is set to another value.

Then coefficients are programmed into the dedicated spare page of Fusion flash memory block (FB) 0 (AFS600 has blocks 0 and 1), from page 50 to 62.

Customers should avoid overwriting these spare pages. An old design generated prior to Libero IDE v8.2 SP1 utilizes these spare pages for Analog System configuration data. Programming an old design to a calibrated device could overwrite these spare pages and corrupt the coefficients. Calibration coefficients of that device would then no longer be available.

On the other hand, programming a design with a calibration block generated from Libero IDE v8.2 SP1 or newer to an uncalibrated device will result in erroneous data from the ADC. To avoid this, customers can pre-program the device with the POPULATION.stp file provided in the Libero IDE v8.2 SP1 release. This programming action populates the dedicated flash memory area for calibration with $m = 1$ and $c = 0$. Then customers can program the device with the design STAPL file.

Calibration IP Deployment

To implement Actel's calibration solution, customers must generate a new Analog System and Flash Memory System using Libero IDE v8.2 SP1 or newer. Actel's calibration IP solution is not available for processor systems that use the CoreAI to interface to the analog block.

Analog System Builder Update

Through the Analog System Builder, customers have an option to deploy a calibration IP block named "CalibIP" into Fusion designs. The CalibIP block is seamlessly inserted into the original Analog System macro, as shown in [Figure 3 on page 6](#). [Figure 3](#) shows only the insertion into a full

Analog System; the same concept applies to the Sequence Only (without SMEV and SMTR stages) and ADC Only (without ASSC, SMEV, and SMTR stages) flows.

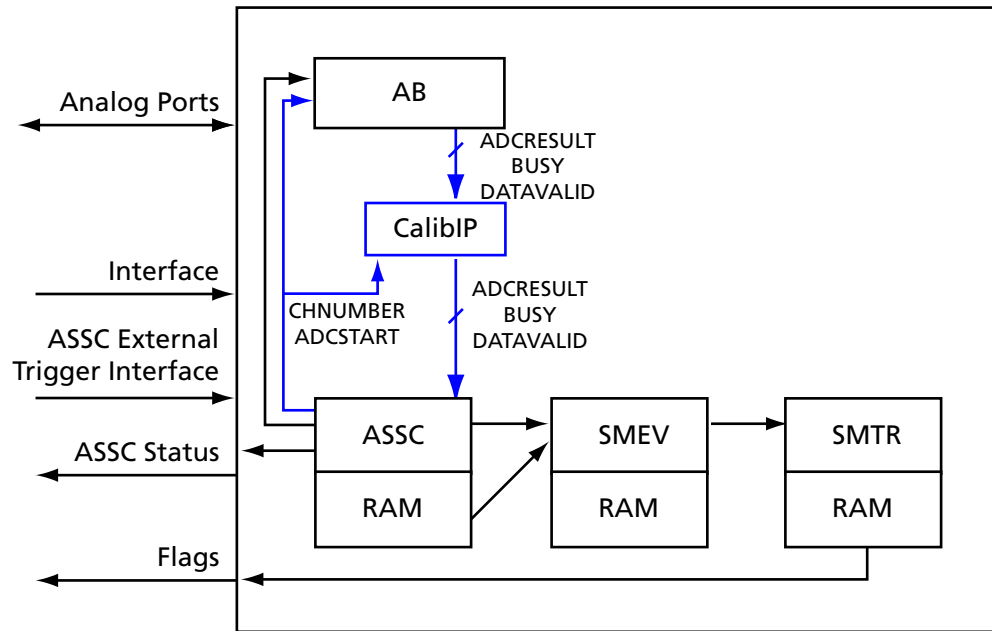


Figure 3 • Full Analog System Macro with CalibIP

During power-up, the initialization state machine, INIT/CONFIG IP, loads the coefficients from the flash memory block into a dedicated SRAM block for the CalibIP core. CalibIP reads the coefficients from the SRAM block and applies the m and c values to the raw ADCRESULT, following [EQ 2 on page 2](#) to generate the calibrated ADCRESULT. The calibrated ADCRESULT then goes through the rest of the process as in the original processing flow.

There are two new ports created at the Analog Block top level to support calibration initialization from the flash memory block:

- INIT_CALIBROM_WEN – Write enable to ROM region, single-bit, active-high
- INIT_CALIBCOEFF_WEN – Write enable to coefficient region, single-bit, active-high

These are write enables for the INIT/CONFIG interface. Connect them to corresponding ports of the flash memory block top level, as shown in [Figure 4 on page 7](#).

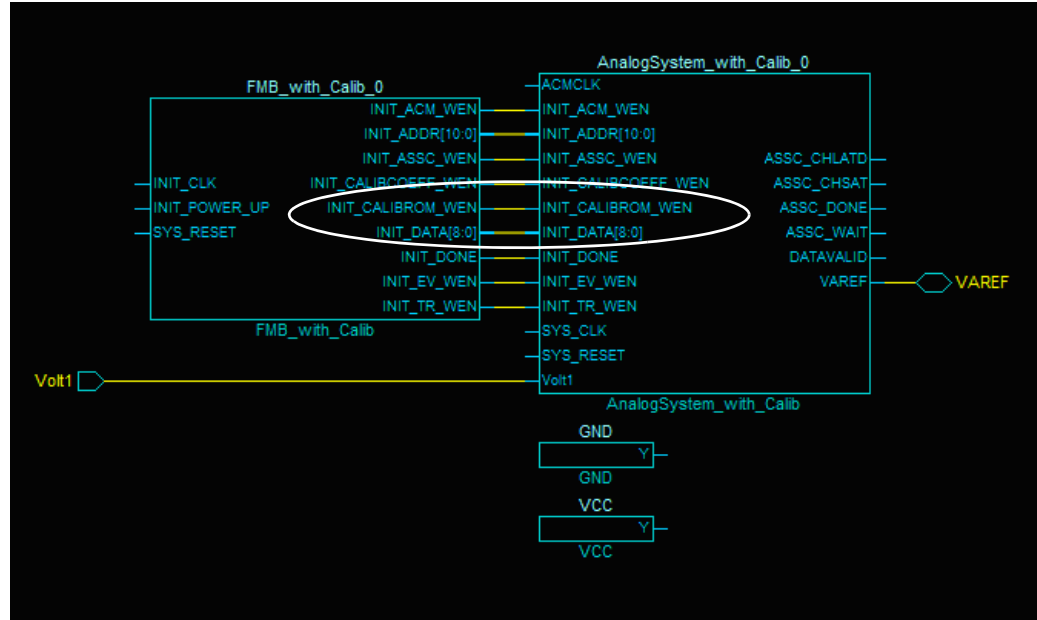


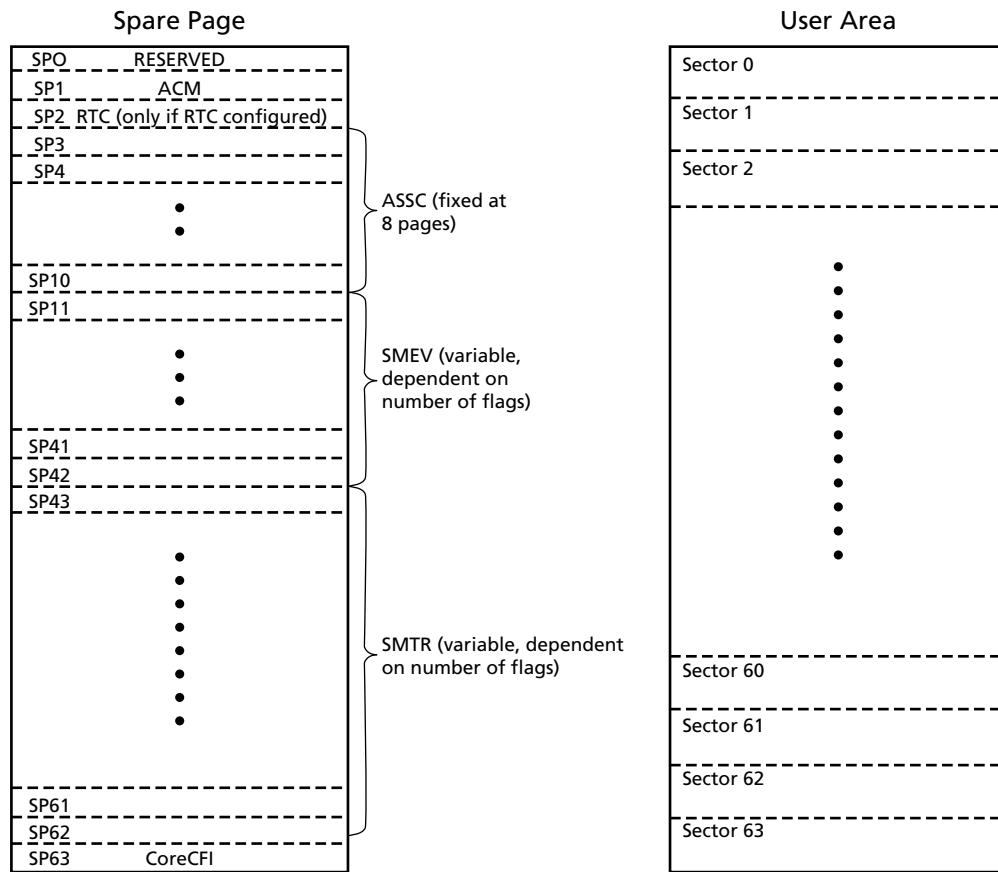
Figure 4 • Connectivity between Analog System Block and Flash Memory Block

Flash Memory System Builder Update

Inside the Flash Memory System Builder (FMSB), customers can generate an analog client to properly initialize the Analog System macro with CalibIP deployed. In addition to the regular Analog System configuration data partition, FMSB also creates two other partitions for the analog client: one for the coefficients' storage (CALIBCOEFFICIENT), from spare page 50 to 62, and one for a lookup table (CALIBROM) that records which channel and prescaler level need to be calibrated, from spare page 43 to 48.

Because of the new calibration coefficients' storage partition, the SMTR configuration data is assigned to flash memory block sector 63, from page 2,016 through 2,047 (or as addresses: 0x3F000 through 0x3FF80). SMTR uses up to 32 pages. The actual number of pages used in this sector depends on whether (and how many) flags are used in the Analog System design. The Flash Memory System Builder prevents customers from assigning any other clients to these pages.

The flash memory maps prior to and after the Libero IDE v8.2 SP1 release are shown in [Figure 5](#) and [Figure 6](#) on page 9.



Flash Memory Block = 64 Sectors
Sector = 32 Pages and 1 Spare Page

Figure 5 • Flash Memory Map Prior to Libero IDE v8.2 SP1

Design Flow and Tips

For calibrated Fusion devices, there are several implementation scenarios.

Scenario 1: Brand New Design

Follow the regular design flow to implement the Actel calibration solution in a new design:

By default, the calibration IP is enabled in the Analog System macro, and the flash memory block initializes the IP. The Designer software places the corresponding analog client in flash memory block 0.

The content of the memory file (*.mem) is different from that of the embedded flash configuration file (*.efc). The *.mem file produced by the Flash Memory Builder for simulation purposes is populated with $m = 1.0$ and $c = 0$ for all channels and all prescaler combinations. CalibIP can function appropriately during simulation. The *.efc file for programming file generation does not include the m and c content because the coefficients are pre-programmed into the device during production test.

To disable the calibration IP, uncheck **Include calibration IP** in the Advanced Options of the Analog System Builder, as shown in Figure 7.

For a calibration-enabled design, when **Bypass calibration on saturated ADC input** is selected, the saturated ADC result is passed to the next level of computation without calibration. If unchecked, the saturated ADC result is calibrated before it is passed to the next level.

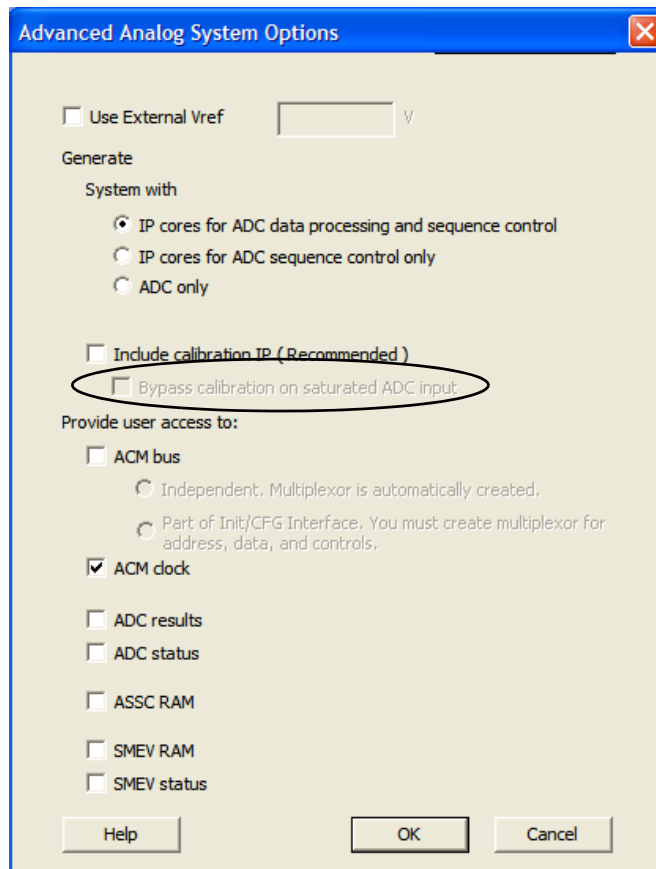


Figure 7 • Disable CalibIP from Advanced Options (Libero IDE v8.2 SP1)

Scenario 2: Update Existing Design to Implement Calibration Solution

To update existing Fusion designs and utilize the Actel calibration solution, take the following steps to regenerate the design:

1. Open the design in Libero IDE v8.2 SP1 or newer.
2. Regenerate the Analog System macro in Analog System Builder.
Open **Advanced Options**, select the **Include calibration IP** option, then regenerate the macro.
3. Regenerate the flash memory block.
4. Make sure the additional ports (INIT_CALIBROM_WEN and INIT_CALIBCOEFF_WEN) are properly connected, either through SmartDesign (Figure 8) or HDL coding.

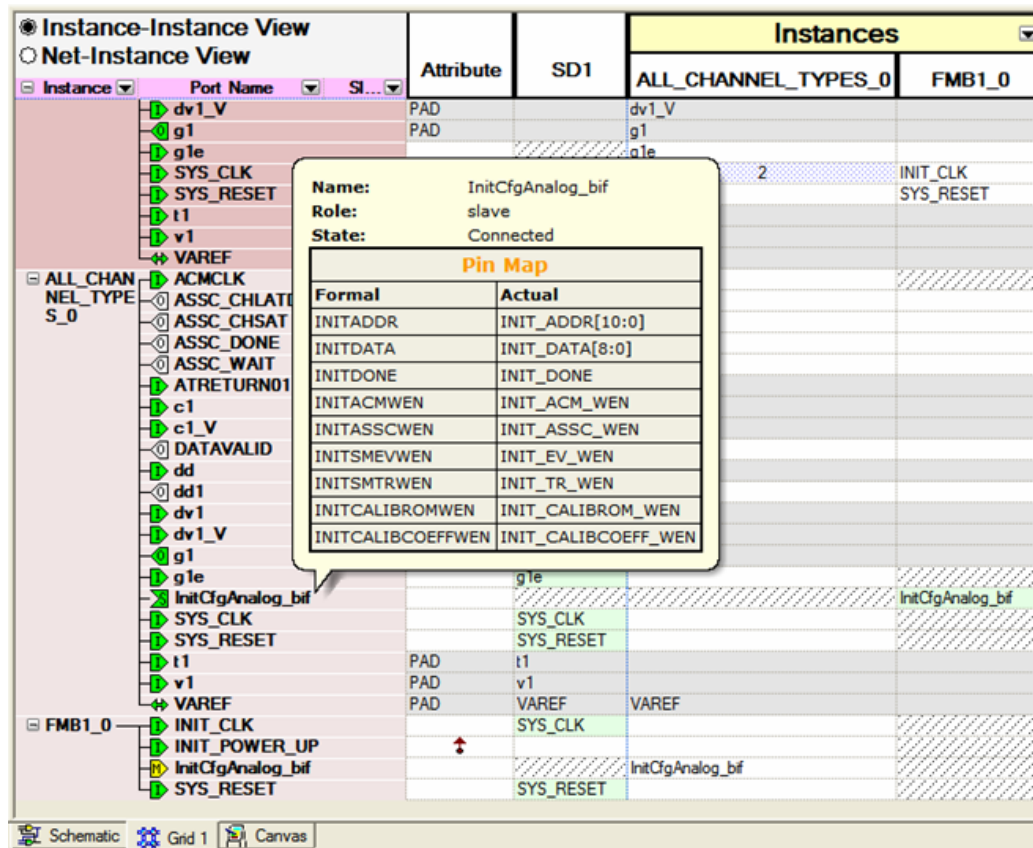


Figure 8 • SmartDesign Connectivity Grid in Libero v8.2 SP1

Go through the rest of the regular design flow (synthesis, compile, and layout with proper simulation and timing analysis).

Scenario 3: Existing Design for Firmware Image Update Only

To update the firmware image in the existing design without using the calibration IP, regenerate the Flash Memory Block. Then go through the rest of design flow (synthesis, compile, and layout with proper simulation and timing analysis).

Scenario 4: Maintain Existing Design in New Software Release without Using Calibration Solution

Actel recommends that all customers regenerate the Analog System Block and the flash memory block in Libero IDE v8.2 SP1 or newer software releases, unless the Analog System Block utilizes less than 20 channels and less than four flags per channel.

Programming a calibrated device with designs generated prior to Libero IDE v8.2 SP1 can overwrite and corrupt the pre-programmed coefficient data in the dedicated flash memory partition. The FlashPro software released with Libero IDE v8.2 SP1 detects whether there is a memory map overlap. If there is a memory overlap, FlashPro cancels the programming action and asks the user to regenerate the Analog System.

To program a design with calibration implemented to a targeted device that is uncalibrated, pre-program the device with the POPULATION.stp file provided by Actel. This programming action populates the dedicated flash memory area for calibration with $m = 1$ and $c = 0$. Then program the device with the design STAPL file.

Utilization and Performance

The total RAM block and core tile utilization to implement CalibIP and the corresponding initialization process is listed in Table 1. CalibIP and other IPs infer registers with enable. When these registers have a SET or RESET signal, assign the SET or RESET signal to a global resource to make sure that the register remains a one-tile implementation (NOT split into two tiles).

Table 1 • Calibration Implementation Utilization Report

RAM Block	Tile Count for CalibIP	
	Optimized for Area	Optimized for Speed
1	363	453

The CalibIP performance is listed in Table 2.

Table 2 • CalibIP Performance Report

Speed Grade	CalibIP Performance (MHz)	
	Optimized for Area	Optimized for Speed
Std.	45	57
-2	75	96

The performance of CalibIP is only limited by the latency introduced by the Compute Block. The Compute Block adds a latency of 14 clock cycles. For example, 14 clock cycles of a 40 MHz system clock is 0.35 microseconds. With calibration implemented, you can expect the ADC result 0.35 microseconds later than in a design without calibration implementation. The sampling rate is degraded by 2%.

Improvement from Actel Calibration Solution

Table 3 shows typical error using Actel's calibration solution.

Table 3 • Fusion Analog System Typical Error with CalibIP Deployed

Input Voltage (V)	Calibrated Typical Error per Positive Prescaler Setting ¹ (%)							Direct ADC ^{2, 3} (%)
	16 V (AT)	16 V (12 V) (AV/AC)	8 V (AV/AC)	4 V (AT)	4 V (AV/AC)	2 V (AV/AC)	1 V (AV/AC)	VAREF = 2.56 V
15	1							
14	1							
12	1	1						
5	2	2	1					
3.3	2	2	1	1	1			
2.5	3	2	1	1	1			1
1.8	4	4	1	1	1	1		1
1.5	5	5	2	2	2	1		1
1.2	7	6	2	2	2	1		1
0.9	9	9	4	4	3	1	1	1

Notes:

1. Requires enabling Analog Calibration in the Actel tool flow.
2. Direct ADC mode using an external VAREF of $2.56V \pm 4.6mV$, without Analog Calibration macro.
3. For input greater than 2.56 V, the ADC output will saturate. A higher V_{AREF} or prescaler usage is recommended.

Microprocessor-Based Design Flow

In a microprocessor-based design flow, designers can use CoreAI (Analog Interface) to interface and control the analog peripherals within the Fusion device family. Designers using Core8051, CoreMP7, or Cortex™-M1 with CoreAI can take advantage of the CoreAI Driver (provided in C code) to support the calibration features.

The CoreAI driver provides a set of Application Program Interface (API) functions to support different calibration modes and automatically calculate the final calibrated value, based on the m and c coefficient stored in the spare page of the Fusion flash memory block.

Currently, the calibration scheme only supports voltage monitor applications (AVx pins) and is only needed for prescaled voltage inputs. If direct analog input sampling accuracy is well within 1%, the Actel calibration solution does not offer any additional benefits. CoreAI driver must be used with CoreAI version 2.1 (or higher) and CoreAhbNvm version 1.3.135 (or higher). Refer to the *CoreAI Driver User's Guide* for more information.

Performing System-Level Calibration Using Fusion

Previous sections of this document describe the general approach to calibration using the offset-only and offset-plus-gain approaches, and provided a detailed explanation of Actel's calibration solution for Fusion voltage input signals. In addition to this solution, users may desire calibration of temperature and current inputs, as well as calibration of the entire system working together. A recommended approach to accomplishing these tasks is provided below. This methodology may be added in the user's design on top of the device-level calibration solution.

The "Calibration Measurements" section on page 3 explains how the calibration coefficients, as described in EQ 1 and EQ 2 on page 2, are calculated. EQ 1 and EQ 2 on page 2 (depending on the calibration method used) are implemented using an adder (one-point calibration) or a combination of an adder and a multiplier (two-point calibration), as shown in Figure 9.

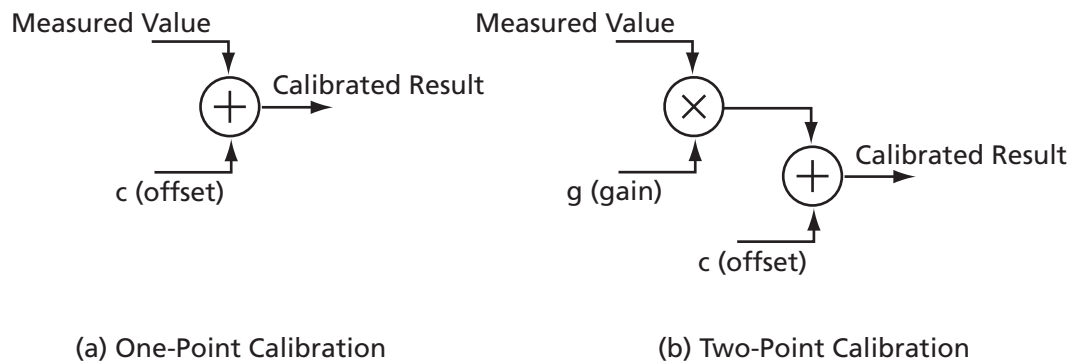


Figure 9 • Implementation of One-Point and Two-Point Calibration

The calibration coefficients (m and c in Figure 9 on page 14) can be stored in the nonvolatile flash memory of each Fusion device. Therefore, inside the flash memory architecture, different memory addresses can contain the calibration coefficients for each channel in the design. Depending on which channel in the design is performing the measurement at the time, appropriate calibration coefficients can be fetched and fed into the adder and/or multiplier. For details on writing and reading to the Fusion flash memory block, refer to the Embedded Flash Memory chapter of the *Fusion FPGA Fabric User's Guide*.

Where and how the adder and multiplier are implemented depends highly on the application and the user's design. Generally, there are three ways designers can implement the arithmetic functions in Figure 9 on page 14 to produce the calibrated results of measurement. The following explains each of these implementations and their pros and cons:

Implementing a Dedicated Adder and Multiplier Using FPGA Core Gates

Pros

- High speed
- Efficient for one-point calibration

Cons

- Multiplier implementation consumes large number of gates

Using the Design's Microprocessor/Microcontroller ALU to Perform Calibration Calculations

Pros

- Saves FPGA gate resources compared to implementing dedicated multiplier

Cons

- May slow down microprocessor's performance depending on the overall sampling rate

Implementing the Numerical Calculations in Application Software

Pros

- Saves FPGA gates

Cons

- Depending on the application, may take up a lot of bandwidth from the host processor
- Only suitable for applications where there is software communicating with hardware

Conclusion

Designers use calibration to increase the accuracy achievable in applications involving analog components. Actel Fusion mixed-signal FPGAs offer the capability of measuring analog voltage, current, and temperature. If customers require more accuracy than is inherent in Fusion FPGAs, calibration techniques can be used to achieve these requirements. Fusion FPGAs offer the advantage of having the calibration design and coefficients programmed into the FPGA itself without a need for any external components. This document discusses the typical calibration techniques and the implementation of Actel calibration solutions for Fusion FPGAs. The result shows that with the Actel calibration implementation, customers can achieve 1% ADC sampling accuracy for all Fusion devices and all channels.

Related Documents

Datasheets

Fusion Family of Mixed-Signal Flash FPGAs

http://www.actel.com/documents/Fusion_DS.pdf

User's Guides

Fusion FPGA Fabric User's Guide

http://www.actel.com/documents/Fusion_UG.pdf

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (51900161-3*)	Page
51900161-3/6.08	The " Microprocessor-Based Design Flow " was added.	13
51900161-1/2.08	This statement was added to the " Calibration IP Deployment " section: Actel's calibration IP solution is not available for processor systems that use the CoreAI to interface to the analog block.	5
	In the " Performing System-Level Calibration Using Fusion " section, a reference to the Fusion Handbook was added.	13
51900161-0/2.07	Please read the document very carefully. A lot of helpful and useful information was added to the document.	N/A
	The " Introduction " section was updated.	1
	The heading title " Calibration Measurements " section is new and all subsections were significantly updated. Please note the variables in all equations were changed. In addition, the variable g was changed to m throughout the document.	3
	The " Actel Calibration Solution " section and all subsections are new.	5
	The heading title "Implementing Calibration Design" was changed to " Performing System-Level Calibration Using Fusion " section. In Figure 9 • Implementation of One-Point and Two-Point Calibration , the m was changed to g.	13

Note: *The part number is located on the last page of the document.

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www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA

Phone 650.318.4200

Fax 650.318.4600

Actel Europe Ltd.

River Court, Meadows Business Park
Station Approach, Blackwater
Camberley Surrey GU17 9AB
United Kingdom

Phone +44 (0) 1276 609 300

Fax +44 (0) 1276 607 540

Actel Japan

EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan

Phone +81.03.3445.7671

Fax +81.03.3445.7668

<http://jp.actel.com>

Actel Hong Kong

Room 2107, China Resources Building
26 Harbour Road
Wanchai, Hong Kong

Phone +852 2185 6460

Fax +852 2185 6488

www.actel.com.cn