

FlashPro4 Backward Compatibility with FlashPro3 and Using FlashPro4 PROG_MODE for 1.5 V Programming of ProASIC3L, IGLOO V2, and IGLOO PLUS V2 Devices

FlashPro4 Backward Compatibility with FlashPro3

FlashPro4 has been announced as backward compatible with FlashPro3; however, there is one significant difference between FlashPro4 and FlashPro3, which ordinarily will not cause any problems.

On FlashPro3, pin 4 of the JTAG header has no connection. On FlashPro4, pin 4 of the JTAG header has a PROG_MODE output drive signal (Figure 1). The PROG_MODE signal toggles between programming and normal operation. During programming, the customer can use PROG_MODE to turn on an external 1.5 V supply for programming. This is required for ProASIC[®]3L, IGLOO[®] V2, and IGLOO PLUS V2 devices. They can operate at 1.2 V, but must be programmed with a VCC core voltage of 1.5 V. A simple regulator circuit for implementing this function is shown in Figure 2 on page 2.

TCK	1	2	GND
TDO	3	4	NC (FlashPro3/3X); PROG_MODE (FlashPro4)
TMS	5	6	VJTAG
VPUMP	7	8	TRST
TDI	9	10	GND

Figure 1 • FlashPro3/FlashPro4 JTAG Header Pin Assignments

The PROG_MODE signal is not a regular I/O but is an open drain signal with a weak pull-up. Users may mistakenly believe this is a regular I/O that can drive 24 mA, which is not the case. The PROG_MODE signal is intended to drive an N- or P-Channel MOSFET to control the output of the regulator between the programming voltage of 1.5 V and normal operation voltage of 1.2 V for the above stated devices.

Pin 4 on FlashPro4 programmers **MUST NOT** be connected or used for anything other than its intended purpose of driving the PROG_MODE signal into a MOSFET. **Actel has found that some FlashPro3 users have the pin 4 connection trace on the board grounded or attached to a positive 3.3 V power supply. When FlashPro4 is used with this same header, either FPGA programming or software loading/debug with SoftConsole is inhibited. As a workaround, the user can cut the wire of the ribbon cable that connects to pin 4 of the FlashPro4 header.**

1.5 V Programming of ProASIC3L, IGLOO V2, and IGLOO PLUS V2 Devices Using FlashPro4 PROG_MODE

Applications that use ProASIC3L, IGLOO V2, and IGLOO PLUS V2 devices powered by a 1.2 V supply must have a mechanism that switches the core voltage from 1.2 V to 1.5 V during in-system programming (ISP). There are several possible solutions to this problem. Actel's recommended solution utilizes a linear voltage regulator, a resistor voltage divider, and an N-Channel digital FET to set the appropriate VCC voltage, as shown in Figure 2 on page 2.

The main component of Actel's recommended circuit is the Linear Tech LTC3025 Linear Voltage Regulator. The output voltage of the LTC3025 on the OUT pin is set by the ratio of two external resistors in a voltage divider. The LTC3025 adjusts the voltage on the OUT pin to maintain the ADJ pin voltage at 0.4 V (referenced to ground). By using an R38 value of 40.2 KOhm and an R37 value of 80.6 KOhm, the output voltage on the OUT pin is 1.2 V. By putting a 107 KOhm voltage for R44 in parallel with R38, the linear regulator will put 1.5 V on the OUT pin. The OUT pin can then be used as a switchable source for the VCC supply. Refer to the LTC3025 Linear Voltage Regulator datasheet for more information.

An N-Channel digital FET is used to enable and disable R44. This FET is controlled by the PROG_MODE signal driven by the FlashPro4 programmer. During programming of the device, the PROG_MODE signal is driven High by the FlashPro4, and turns the N-Channel digital FET ON. When the FET is ON, R44 becomes enabled as a parallel resistance to R38, which will force the regulator to set OUT to 1.5 V.

When the FlashPro4 is connected and not programming, or when the FlashPro4 is not connected, the pull-down resistor R10 will pull the FET input signal Low. When this signal is Low, the N-Channel digital FET is opened and R44 is not part of the resistance seen by the LTC3025. The new resistance momentarily changes the voltage value on the ADJ pin, which in turn causes the output of the LTC3025 to compensate by setting OUT to 1.2 V. The FPGA device will now run in the regular active mode at the required 1.2 V core voltage.

Example Circuit

Figure 2 shows an example switching circuit using PROG_MODE.

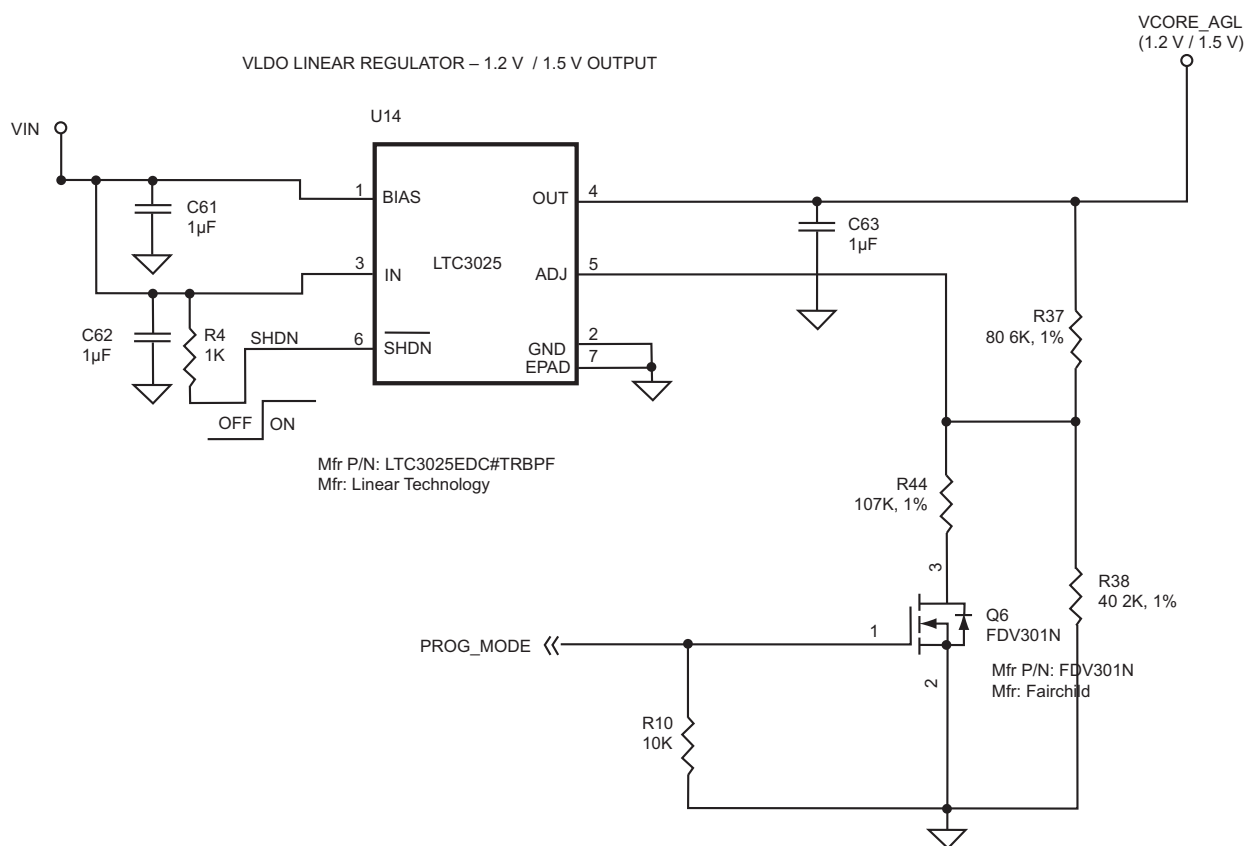


Figure 2 • Example Switching Circuit Using PROG_MODE with the LTC3025

Conclusion

Actel's ProASIC3L, IGLOO V2, and IGLOO PLUS V2 low power FPGAs offer 1.2 V core operation; however, they must be programmed with a core voltage of 1.5 V. If the device is operating at 1.2 V, there must be a way for the core voltage to switch from 1.2 V to 1.5 V during programming. The circuit explained in this document illustrates one simple, cost effective way of handling this requirement. A PROG_MODE signal from the FlashPro4 programmer allows the circuit to sense when programming is in progress, enabling it to switch to the correct core voltage.

The pin 4 PROG_MODE signal coming from FlashPro4 MUST NOT be connected to any other circuitry on the JTAG traces on the board or the FlashPro4 functionality may be inhibited.

Disclaimers

If you are using the Linear Technology LTC3025 regulator as shown in [Figure 2 on page 2](#), ensure that the manufacturer's guidelines are correctly followed. It is important to follow the correct guidelines to ensure the solution works.

If you are using a different regulator, please ensure the following:

1. The logic of the PROG_MODE pin translates to the correct change in voltage. It may be the opposite of what is shown in [Figure 2 on page 2](#). In that case you may need to add an inverter on the PROG_MODE pin.
2. The manufacturer indicates that it is acceptable to change the feedback resistance dynamically on the board without the need of doing a power cycle.
3. No extra ripple is generated on the output of the regulator if the feedback resistance is changed dynamically.

The regulator example in [Figure 2 on page 2](#) has been tested and utilized in various Actel board designs; however, Actel customers are fully responsible for the final regulator design, functionality, and validation.



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