

Synplify DSP AE Design Flow

Quickstart and Design Tutorial

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Introduction

This Quickstart and tutorial assumes that you already have the Mathworks Matlab®/Simulink® software and license. Visit http://www.mathworks.com/products/product_listing/index.html for more information. Synplify DSP requires the installation of Matlab/Simulink and can only be launched from the Matlab/Simulink tools.

Synplify DSP AE (Actel Edition) Software and License Availability

Synplicity® Synplify DSP AE software and licenses are available free to Actel customers from the Actel website.

Using Synplify DSP AE with Synplify/Synplify Pro AE Synthesis

Although Synplify AE synthesis can be used with Synplify DSP AE, it may not achieve the best possible design performance. Actel recommends use of Synplify Pro AE only for the best possible design results.

Device Support

Synplify DSP AE v.3.4.1A supports the following device families:

- Fusion
- ProASIC®3/E
- ProASIC^{PLUS}®
- Axcelerator®

License Installation and Setup

Setting up the license for Synplify DSP requires careful consideration. Synplify uses a “server-based node-locked” license system for DSP that works differently from the Libero IDE “node-locked” license system. When both are used, pay careful attention to the installation and setup of the DSP license. Synplify DSP does not run standalone, and can only be launched from within the Mathworks Matlab/Simulink application. If the DSP license is not installed and set up correctly, Synplify DSP can be launched, but full use of the tool is not possible.

Installing the Synplify DSP License

1. Create a folder called **Flexlm** on your C: drive.
2. Save the attached license file in the *Flexlm* folder with the filename **license_dsp.dat**. This is necessary because your Libero IDE tools are stored in the *license.dat* file. The DSP license **MUST** be stored separately with a different file name from the Libero IDE license.
3. Open the **license_dsp.dat** file with Notepad or Wordpad.
4. In the line,


```
SERVER <put.hostname.here> 123456789012 TCP:1702,
```

 replace **<put.hostname.here>** with the name of your Windows PC, found on the Computer Name tab of your System Properties information. Do not include the brackets.
5. Save the **license_dsp.dat** file and close it.

Setting Up the Synplify DSP License

1. Go to **Start>Run**.
2. Browse to the **C:\SynLM** folder. Select, open, and run **lmtools.exe**. The LMTOOLS License Manager is installed as part of a Libero IDE/Synplify software installation.
3. From the **Service/License File** tab, click only the **Configuration using Services** radio button. LMTOOLS License Manager text displays in the window.
4. Click the **Config Services** tab in the LMTOOLS License Manager.
5. In the **Path to the lmgrd.exe file**, browse to **C:/SynLM** and click **lmgrd.exe**. This is the license daemon. The path should be **C:/SynLM/lmgrd.exe**.
6. In the **Path to the license file**, browse to and click **C:/Flexlm/license_dsp.dat**, as described in step 2 of “[Installing the Synplify DSP License](#)” above.
7. In the **Path to the debug log file** field, type **C:\SynLM\serverlog**.
8. Check the **Use Services** check box.
9. Check the **Start at Powerup** check box.
10. Click the **Save Service** button to save this configuration.
11. Click the **Stop/Start/Re-read** tab on the LMTOOLS License Manager.
12. Click the **Start Server** button to start the License Manager.
13. Close the LMTOOLS dialog.

Note: This server should not be running during the installation of Synplify DSP AE.
14. Open the **Control Panel** and double click the **System** icon.
15. In the **Systems Properties** dialog box, left click the **Advanced** page tab.
16. Left click the **Environment Variables** button.
17. Left click the topmost **New** button. **New User Variable** is visible.
18. In the **Variable Name** field, type **SYNPLCTYD_LICENSE_FILE**.
19. In the **Variable Value** field, type **C:\flexlm\license_dsp.dat**.

20. Click **OK**.
21. You are finished with **Environment Variables**. Click **OK** to close.
22. Start MATLAB. Change the working directory to **C:\Program Files\Synplicity\Synplicity_dsp_ae_341A\mathworks**.
Note: Version 341A is in the folder path.
If you had a previous version of Synplify DSP software installed, you must start a new MATLAB session.
23. At the MATLAB command line prompt, type **setup** to execute the setup script (setup.m file) in the working directory. The installation confirms the locations with a Installation Complete popup window.
24. Click **OK** to close the window.
25. Type **syndsproot** at the MATLAB command line to double check the installation. MATLAB shows the Synplify DSP installation path **C:\Program Files\Synplicity\Synplify_dsp_ae_341A**.
Note: Version 341A is in the folder path.
26. Type **path** on the MATLAB command line to show the path where the MATLAB software is installed.
27. Type **syndspver** on the MATLAB command line to show the MATLAB and Synplify DSP version numbers.
28. With Matlab open, you can create a new Simulink model, and the Synplify DSP library should be showing.
29. Follow the [“Tutorial for Using Synplify DSP AE v.3.4.1A with Libero IDE v.8.1”](#) on page 9 to successfully manage a Matlab/Simulink Synplify DSP and Libero IDE design flow.

Tutorial for Using Synplify DSP AE v.3.4.1A with Libero IDE v.8.1

Introduction

Synplify DSP AE translates a design from a higher level algorithm description in Simulink into an encrypted RTL code that can be synthesized using Synplify Pro AE. Synplify DSP also creates an HDL testbench for the design by capturing the stimulus used to test the design within the Simulink environment. This facilitates verification and makes the netlist bit and cycle true, compared to the Simulink model of the DSP design.

Currently Matlab and Simulink (including Synplify DSP) are not integrated in Libero IDE v.8.1. This tutorial gives step-by-step instructions on how to run Synplify DSP and import the design files, testbench, and test vector files into the Libero IDE v.8.1. It also describes the options and settings required by Libero IDE v.8.1 for a smooth design flow.

Synplify DSP AE v.3.4.1A Overall Flow

Figure 2-1 on page 10 shows the overall DSP design flow using MatLab/Simulink and Libero IDE with Synplify Pro AE. Synplify DSP translates the DSP design created in Simulink into encrypted RTL. This encrypted RTL is not recognized by Libero IDE. You must run Synplify Pro AE outside Libero IDE to read this encrypted RTL and convert it to an EDN netlist block. This netlist block is then converted to an HDL block using the `edn2VHDL` (or `end2verilog`) utility available from Libero IDE Designer physical implementation tools. This structural RTL netlist, other HDL files, and testbench, along with the test vectors, can then be imported into the Libero IDE flow that allows a smooth synthesis, simulation, place-and-route, and programming of the design.

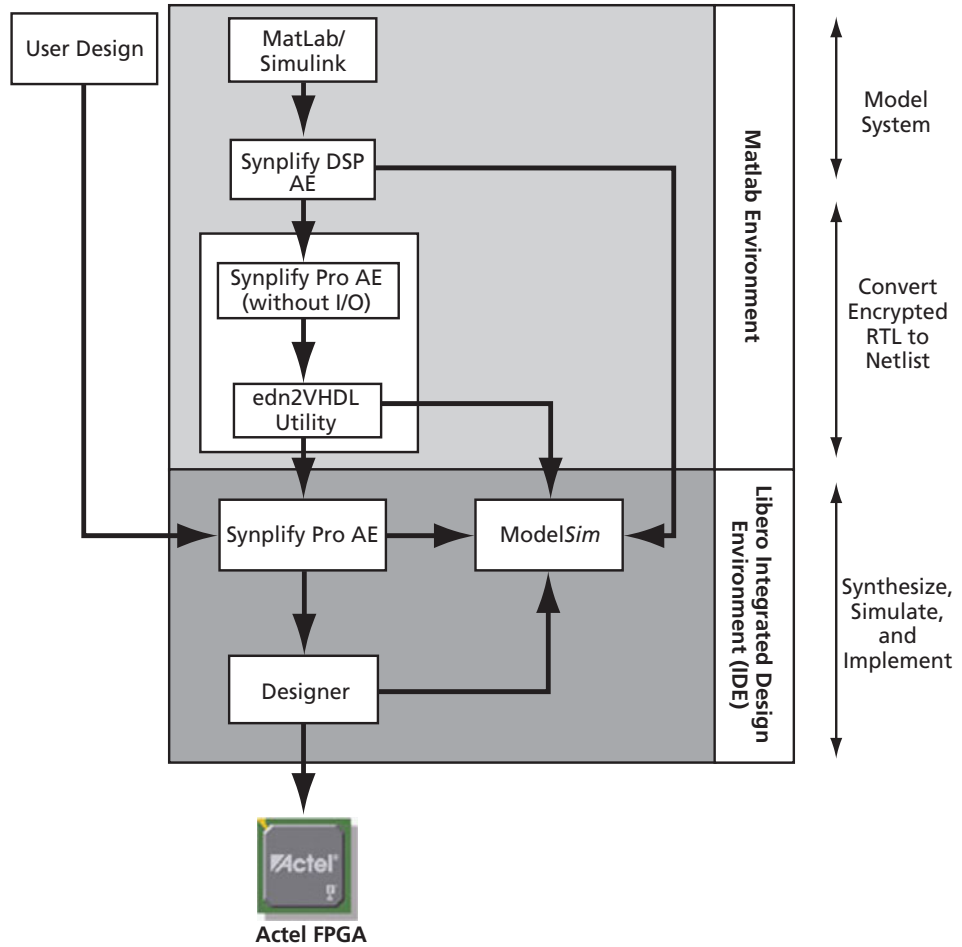


Figure 2-1. Actel DSP Design Flow

Tutorial Steps

The following steps will be followed in this tutorial:

- “Step 1 – Create Encrypted RTL from the DDC Model File”
- “Step 2 – Convert the Encrypted RTL to an RTL Netlist”
- “Step 3 – Create a New Libero IDE Project”
- “Step 4 – Import the RTL, Testbench, and Test Vector Files”
- “Step 5 – Set Up the Simulation Environment and Perform Simulation”
- “Step 6 – Synthesize the Design with Synplify Pro AE”
- “Step 7 – Implement the Design Using Libero IDE Designer Physical Implementation Tools”
- “Step 8 – Perform a Timing Simulation with Back-Annotated Timing”
- “Step 9 – Generate the Programming File”
- “Step 10 – Program and Test the Device”

Steps 1 and 2 will be done in the Matlab environment and the rest of the steps will be done in the Libero IDE. In this tutorial, we will only use a VHDL flow. A Verilog user could follow the same flow.

Step 1 – Create Encrypted RTL from the DDC Model File

This step opens Matlab and creates encrypted RTL using Synplify DSP.

1. Download the `ddc.zip` file from <http://www.actel.com/documents/DDC.zip> to your desktop. Unzip the file, and save ALL items to `C:\demo`. You will need all files and retaining the file names is important.
2. Open Matlab and set the current directory to `C:\demo`.
3. Double-click the `ddc.mdl` file to open the demo model file.

The `ddc.mdl` file is shown in [Figure 2-2 on page 12](#).

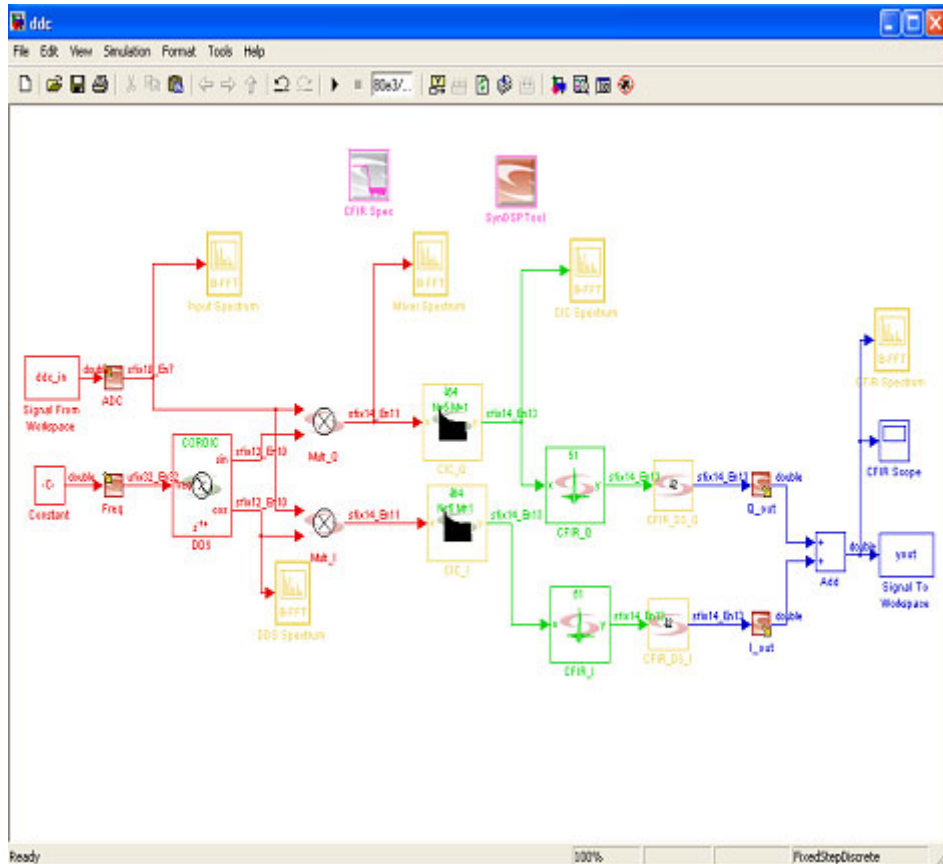


Figure 2-2. DDC Design

4. Double-click the SynDSPTool inside the model file and launch the Synplify DSP AE v.3.4.1A tool, as shown in Figure 2-3.

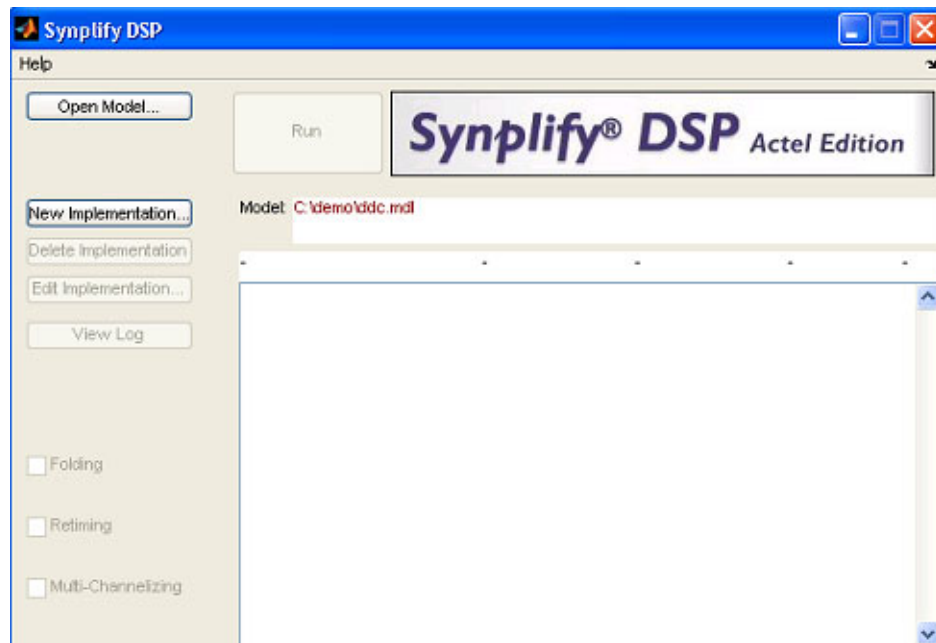


Figure 2-3. Synplify DSP User Interface

5. Select **New Implementation** to open the **Implementation Options** dialog box. Select the following:
 - Device**
 - Vendor: Actel
 - Technology: ProASIC3E
 - Part: A3PE1500
 - Speed: Std
 - RTL**
 - Select the **Generate VHDL** check box
 - Select the **Generate RTL test bench** check box

- Click OK (Figure 2-4) to accept the implementation settings. Figure 2-5 shows the result.

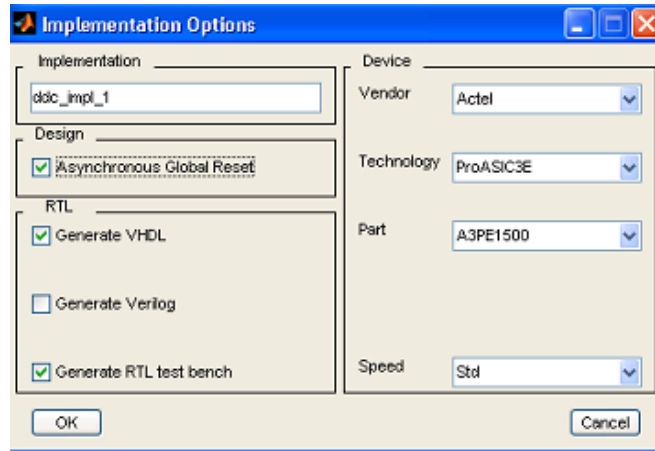


Figure 2-4. Implementation Options Dialog Box



Figure 2-5. Synplify DSP GUI with ddc_impl_1 Implementation

- Click Run and Synplify DSP AE will create encrypted RTL for the model file.

Synplify DSP will create files in the `C:\demo\ddc_impl_1\vhdl` folder, including the encrypted RTL (Figure 2-6).

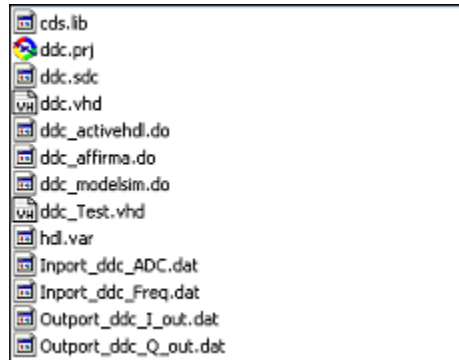


Figure 2-6. Files Generated by Synplify DSP

Step 2 – Convert the Encrypted RTL to an RTL Netlist

This step uses Synplify Pro AE and the Libero IDE Designer `edn2vhdl` utility in the Matlab environment. The encrypted RTL is converted to RTL netlist format.

1. Navigate to the `C:\demo\ddc_impl_1\vhdl` folder.

2. Launch Synplify Pro AE from Matlab, using the following command:

```
>>!<synplify_install>\bin\synplify_pro
```

For example:

```
>>!H:\Synplicity86\fpga_861\bin\synplify_pro
```

3. Open Synplify Pro project `ddc.prj`, which was created in Step 1. This project file has the required family/device settings and disables the I/O insertion in the netlist.

4. Select **Run** to create the EDN file.

Synplify Pro will read the Synplify project file created by Synplify DSP and generate an EDN file, which is placed in the `./rev_1` folder.

5. Navigate to `C:\demo\ddc_impl_1\vhdl\rev_1`.

6. Run the `edn2vhdl` command in Matlab to convert the EDN to a VHDL file:

```
>> !edn2vhdl FAM:ProASIC3E EDNIN:ddc.edn VHDOUT:ddc.vhd ddc
```

This will create the VHDL netlist from the EDN file. The VHDL netlist can be imported into Libero IDE.

7. Close Matlab.

Step 3 – Create a New Libero IDE Project

This step uses the Libero IDE software to create a project for the tutorial design. A Libero IDE project sets the design name, the HDL flavor (VHDL or Verilog), and the tools to be used.

1. Start Libero IDE by double-clicking the **Actel Libero IDE** icon on the desktop.

- From the Project menu, select New Project. This displays the New Project dialog box, as shown in Figure 2-7.

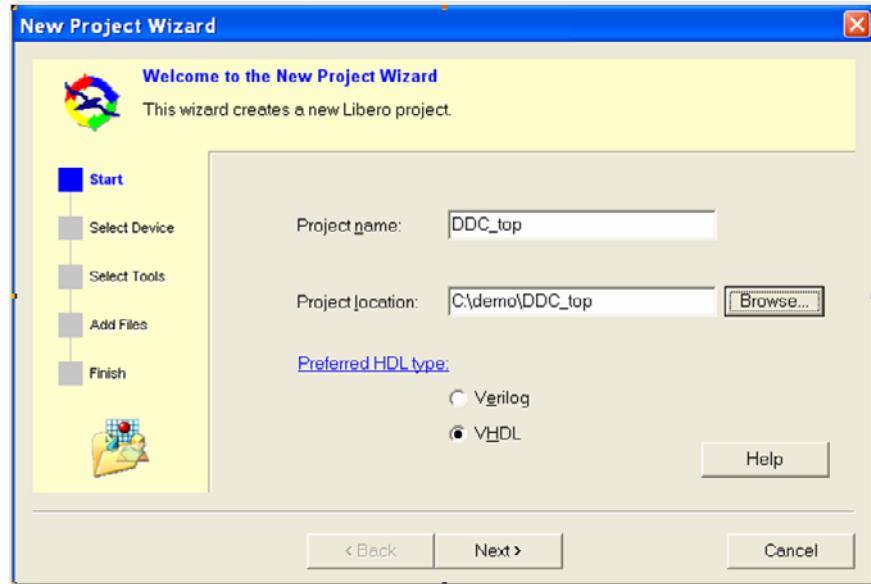


Figure 2-7. Libero IDE New Project Wizard

- Browse to C:\demo location and enter DDC_top in the Project Name field.
- In the Project Location field, verify that the path C:\demo\DDC_top is displayed.
- Select the VHDL radio button in the Preferred HDL type field.
- Click Next. The Family, Die and Package window will appear.
- Select ProASIC3E to access the ProASIC3E family from the Family drop-down list.
- Select the A3PE1500 die and 208 PQFP package (Figure 2-8).

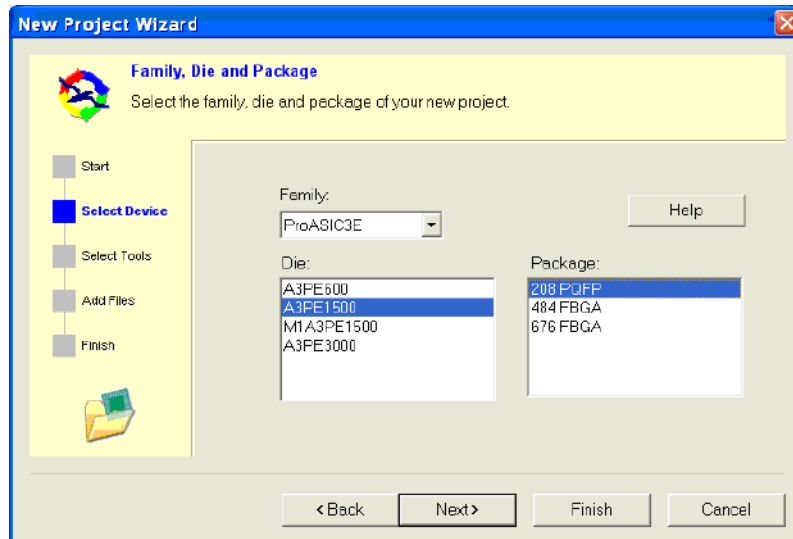


Figure 2-8. Family, Die and Package Dialog Box

9. Select **Next** and choose the appropriate tools settings, if they are not already selected (Figure 2-9). The tools shown in this dialog box will depend upon your installation. If you want to change the default tool settings, refer to the *Libero IDE User's Guide* or Libero IDE online help.

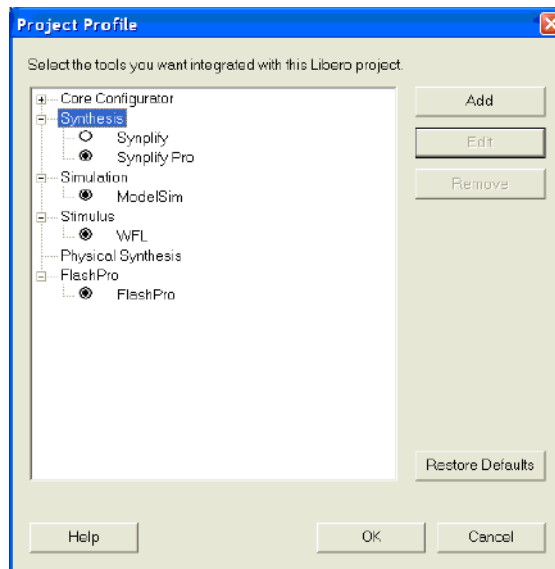


Figure 2-9. Select Integrated Tools Dialog Box

10. Click **Finish**.

The project *DDC_top* will be created and opened in the Libero IDE, as shown in Figure 2-10.

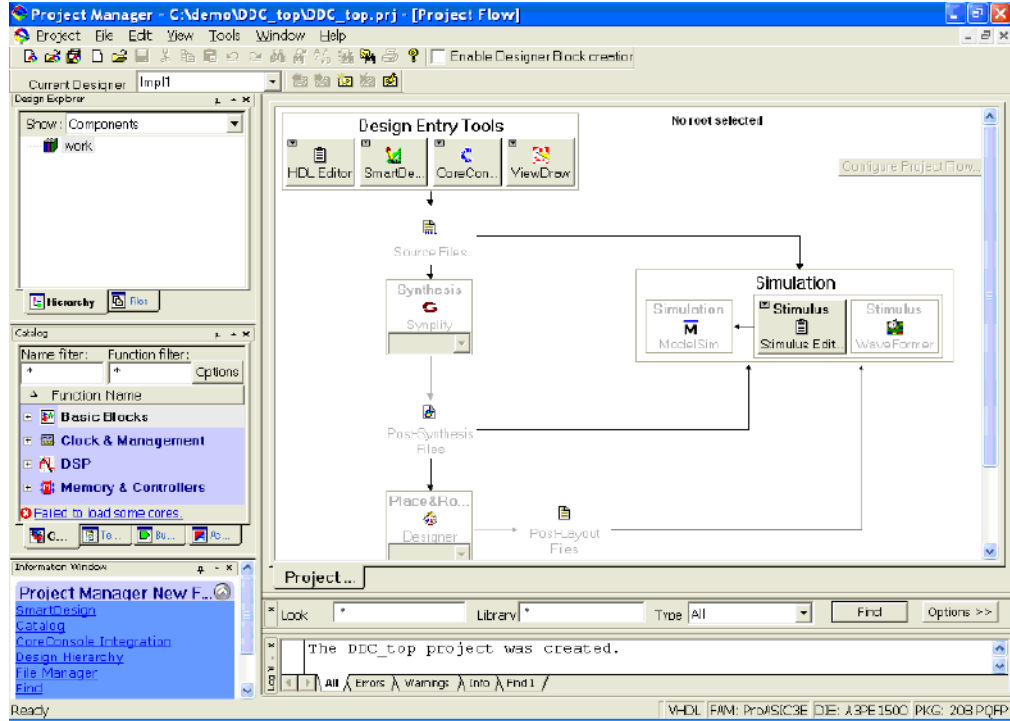


Figure 2-10. Libero IDE Design Flow Window with DDC_top Project

Step 4 – Import the RTL, Testbench, and Test Vector Files

This step imports the RTL, testbench and test vector into Libero IDE.

1. Navigate to the **Files** tab, right click **HDL Source Files**, and select **Import**.

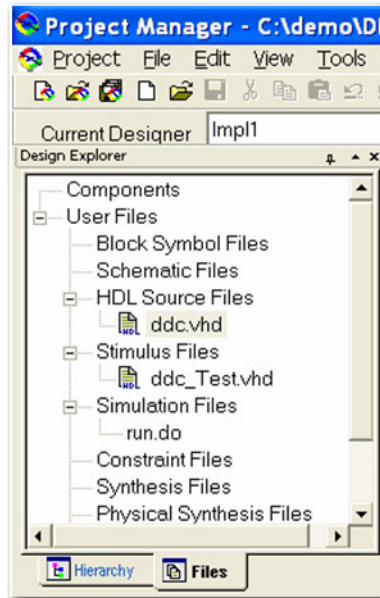


Figure 2-11. Importing DDC_top Project Source Files into Libero IDE

2. Browse to `C:\demo\ddc_impl_1\vhdl\rev_1` and import the `ddc.vhd` file.
3. Right click on **Stimulus Files**. Browse to `C:\demo\ddc_impl_1\vhdl` and import the `ddc_Test.vhd` file.
4. Right click on **Simulation Files**. Browse to `C:\demo\ddc_impl_1\vhdl` and import all the **DAT** files.

In this design tutorial, only the `ddc.vhdl` file generated in Step 2 is used. You can, however, add other files from the folder.

Step 5 – Set Up the Simulation Environment and Perform Simulation

Once the structural RTL, testbench, and test vector files are imported, use *ModelSim* to perform a pre-synthesis simulation.

1. First, you need to associate a stimulus file with the design. This lets the *ModelSim* tool know which testbench to use for the simulation.
2. To set up the stimulus file, right click on `ddc` in the Libero IDE **Design Hierarchy** tab and select **Organize Stimulus** to launch the *Organize Stimulus* window.

3. Add the stimulus file under **Associate Files**, as shown in the Organize Stimulus dialog box in [Figure 2-12](#).

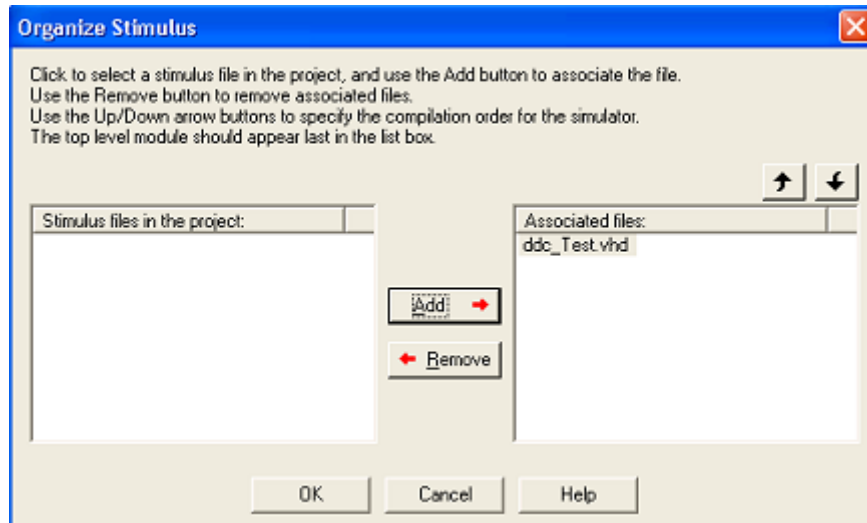


Figure 2-12. Organize Stimulus Dialog Box

- After selecting the stimulus file, set the simulation environment.
4. Select **Settings** from the Project pulldown menu to open to open the Project Settings dialog box ([Figure 2-13 on page 21](#)).
 5. Select the **Simulation** tab and change the following:
Top Level entity name: `test_ddc`
Top Level instance: `i_ddc`
 6. Click **OK** to accept the settings.

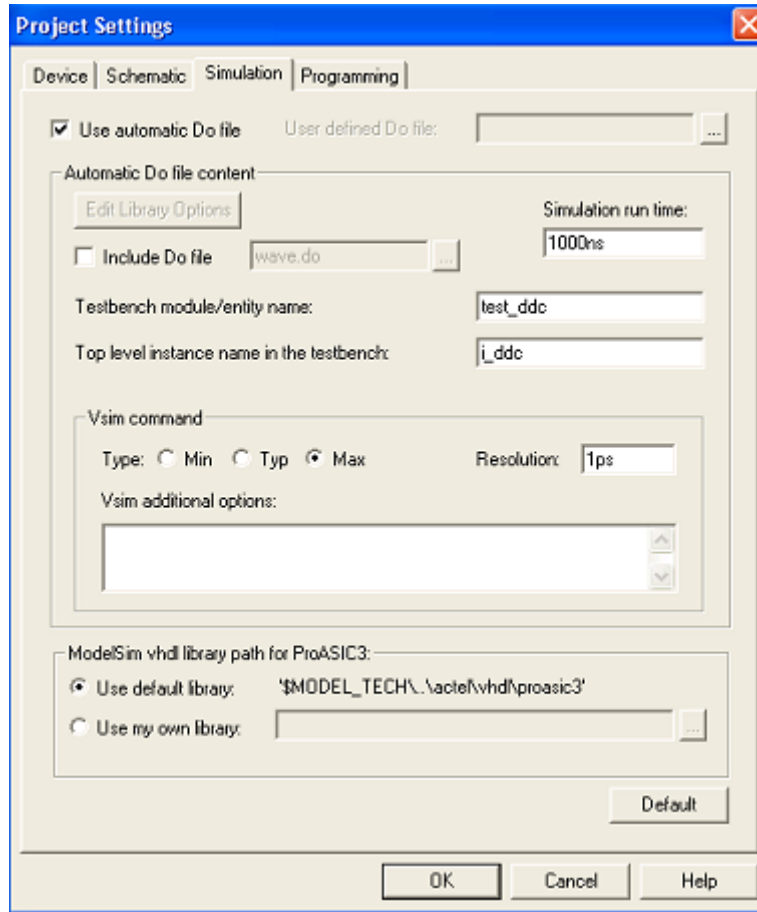


Figure 2-13. Simulation Options Window

Now, start the simulation.

7. Double-click the ModelSim Simulation icon in the Libero IDE Process window, or right click ddc in the Libero IDE Design Hierarchy tab and select Run Pre-synthesis Simulation.

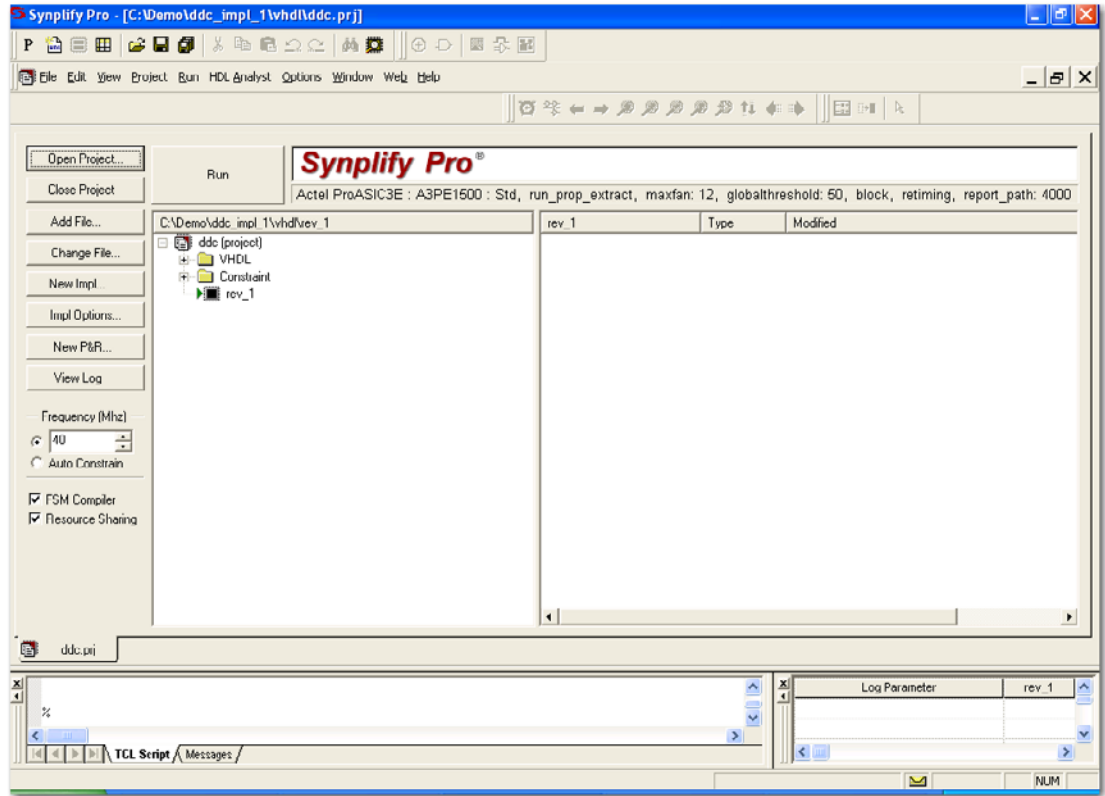


Figure 2-15. Synplify AE GUI

Step 7 – Implement the Design Using Libero IDE Designer Physical Implementation Tools

The next phase is to implement the design in an A3PE1500-PQ208 device using the Actel Designer software.

1. Double-click the Designer **Place-and-Route** icon in the Libero IDE **Process** window, or right-click **ddc** in the **Design Hierarchy** tab of the Design Explorer Window and select **Run Designer**. The Actel Designer application opens and the design file (*ddc.edn*) is automatically read in (Figure 2-16).

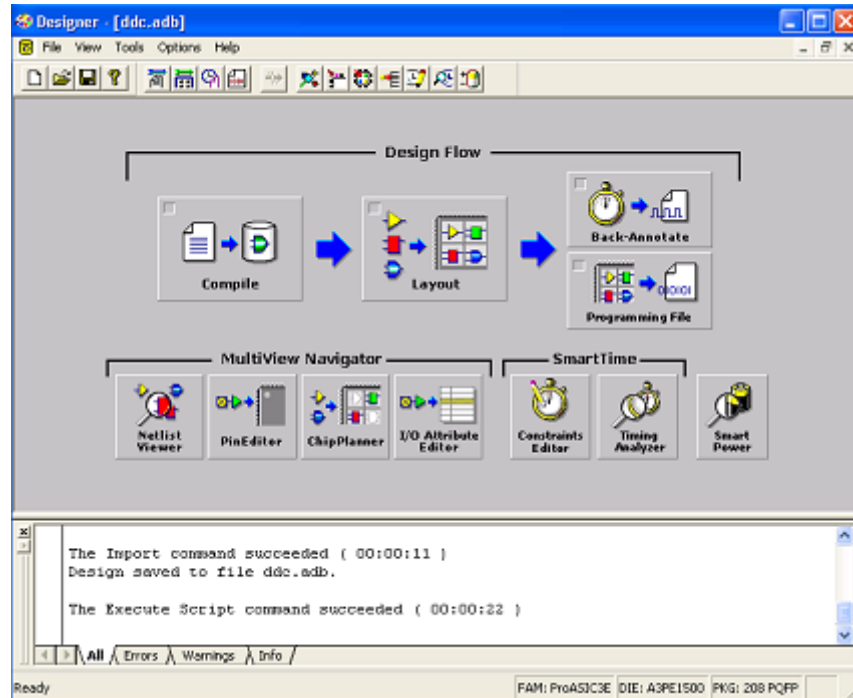


Figure 2-16. Libero IDE Designer User Interface

2. Click the **Compile** button and select the appropriate setting in the device selection wizard.
3. (Optional) Assign pins using **PinEditor** or **I/O Attribute Editor**.
4. From Designer, click the **Layout** button to execute place-and-route. This may take from half an hour to one hour for this large device design.
5. Click the **Back-Annotate** button to generate the back annotated files.
6. Save and close Designer.

Step 8 – Perform a Timing Simulation with Back-Annotated Timing

After completing place-and-route and delay extraction of the design, perform a back-annotated (post-layout) timing simulation with the ModelSim HDL simulator.

Click the ModelSim **Simulation** icon in the Libero IDE **Design Flow** window, or right-click the **TOP** file in the **Design Hierarchy** tab and select **Run Post-Layout Simulation**.

This launches the ModelSim Simulator, which compiles the back-annotated VHDL netlist file and testbench. Scroll in the **Wave** window to verify that the design works correctly. Use the zoom buttons to zoom in and out as necessary.

Step 9 – Generate the Programming File

This step generates the necessary programming file for the selected device, to be used with the FlashPro device programmer.

1. Right click the **ddc** file in the **Design Hierarchy** tab to open Designer. Click the **Programming Files** button to launch the Programming Files generator window. Choose the appropriate option to generate the programming file.
2. The programming file is saved to the Libero IDE project files, appearing in the File Manager under implementation files.

Step 10 – Program and Test the Device

The device is now ready to be programmed and tested.

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call 650.318.4480

From Southeast and Southwest U.S.A., call 650.318.4480

From South Central U.S.A., call 650.318.4434

From Northwest U.S.A., call 650.318.4434

From Canada, call 650.318.4480

From Europe, call 650.318.4252 or +44 (0) 1276 609 300

From Japan, call 650.318.4743

From the rest of the world, call 650.318.4743

Fax, from anywhere in the world 650.318.8044

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the [Actel Customer Support website \(www.actel.com/custsup/search.html\)](http://www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's [home page](http://www.actel.com), at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460

800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. [Sales office listings](#) can be found at www.actel.com/contact/offices/index.html.

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