

Clock Generation and Distribution Design Example for IGLOO[®] and ProASIC[®]3 FPGAs

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General Description

This design example demonstrates the use of the IGLOO and ProASIC3 clock conditioning circuits and phase-locked loops (PLLs) to generate multiple clock signals with different phases and frequencies. In this design, two PLLs are cascaded and configured in dynamic mode, giving the user the ability to externally control the output frequency while the device is operating. The design can be altered by removing a PLL for devices that only support a single PLL.

Design Description

The top-level block diagram of the IP is shown in [Figure 1](#).

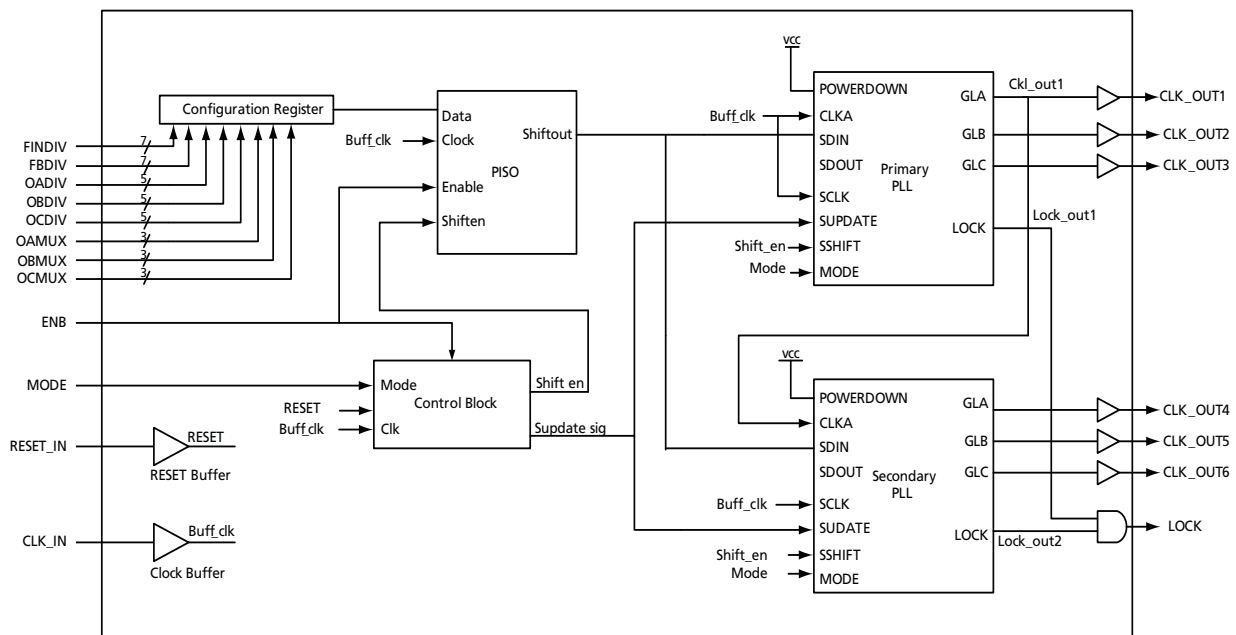


Figure 1 • Top-Level Block Diagram

The generated clocks will be derived from the single input clock CLK_IN. This clock is routed internally using a global clock buffer and global routing resources to the PLL inputs. The parallel-in-serial-out (PISO) is the shift register that converts configuration data for the PLLs from parallel to serial. The control block generates the necessary control signals for the shift register and the PLLs. Two PLLs are cascaded to generate six clock outputs; these PLLs will be referred to as primary PLL and secondary PLL.

The PLLs can be configured in two ways:

- Static configuration, where the output frequency parameters will be hardcoded in the design during design creation in the Libero® Integrated Design Environment (IDE).
- Dynamic configuration, where the output frequency required can be modified on-the-fly.

The selection between the static or dynamic configuration is done with the help of a MODE signal. If the MODE pin is low, static configuration is selected; if the MODE pin is high, dynamic configuration is selected.

Design files for this design example can be downloaded from the Actel website:

www.actel.com/download/rsc?f=Clock_Generation_Distribution_DF.

Static Mode

In static mode, the PLLs are loaded with hardcoded parameters: the output frequency will remain constant for a given frequency input. Table 1 shows VCLK values for an input frequency of 20 MHz.

Table 1 • Static Mode Outputs for 20 MHz Input Clock

Clock Output	Frequency
CLK1	10 MHz
CLK2	15 MHz
CLK3	25 MHz
CLK4	30 MHz
CLK5	35 MHz
CLK6	40 MHz

Dynamic Mode

In dynamic mode, the required parameters are driven through an external interface. Detailed information about the PLL configuration parameters and methodologies can be found in the *IGLOO FPGA Fabric User's Guide*, available at www.actel.com/documents/IGLOO_UG.pdf.

The configuration bits are serially loaded into a PLL through the SDIN port with the least significant bit (LSB) as first bit. To configure the PLLs with new parameters, set the control signal, SSHIFT, low and set SUPDATE high. After the configuration is done, deassert the SUPDATE signal (low). To simplify PLL configuration in this design, the control block manages the SSHIFT and SUPDATE signals to the PISO block and to the PLLs when ENABLE is high (active). The ENABLE signal also enables the PISO block.

Once 80 configuration bits are shifted to the PLL, the control logic will assert the SUPDATE signal and deassert the SSHIFT signal to enable the new configuration. When both the primary and the secondary PLLs lock to the reference frequency, the LOCK signal is asserted (high). After the LOCK signal is high, all the frequencies will be available and stable.

Note: The PLLs must be configured with valid parameters. Refer to the device handbooks for further details.

In this design, delays and phase shifts are not programmable and they are hardcoded to value 0x1000000017. If required, these bits can also be taken out as an input to design to provide programmability.

For dynamic mode, the output clock frequency is calculated based on EQ 1.

$$\text{Clock output} = \text{PLL input frequency} \times \frac{\text{feedback divisor value}}{\text{input divisor value} \times \text{multiplier value}}$$

EQ 1

The output clock frequencies for the clock outputs are:

$$\text{CLK_OUT1} = \text{Fref_clk} \times \text{FBDIV} / (\text{FINDIV} \times \text{OADIV})$$

$$\text{CLK_OUT2} = \text{Fref_clk} \times \text{FBDIV} / (\text{FINDIV} \times \text{OBDIV})$$

$$\text{CLK_OUT3} = \text{Fref_clk} \times \text{FBDIV} / (\text{FINDIV} \times \text{OCDIV})$$

$$\text{CLK_OUT4} = \text{CLK_OUT1} \times \text{FBDIV} / (\text{FINDIV} \times \text{OADIV})$$

$$\text{CLK_OUT5} = \text{CLK_OUT1} \times \text{FBDIV} / (\text{FINDIV} \times \text{OBDIV})$$

$$\text{CLK_OUT6} = \text{CLK_OUT1} \times \text{FBDIV} / (\text{FINDIV} \times \text{OCDIV})$$

Where

CLK_OUT n denotes the different clock outputs

Fref_clk is the input clock reference for the primary PLL

FBDIV is the feedback divisor value for the PLL

FINDIV is the input divisor value

OADIV is the multiplier value for clock output A

OBDIV is the multiplier value for clock output B

OCDIV is the multiplier value for clock output C

Note: The first three outputs are from the primary PLL and the last three outputs are from the secondary PLL.

Interface Description

Table 2 describes the interface signals for the IP.

Table 2 • Interface Details

Signal	Direction	Description
RESET	Input	Active low reset signal for the design
MODE	Input	Low – Static configuration High – Dynamic configuration
ENB	Input	Active high enable for loading the new configuration bits in the design
CLK_IN	Input	Input reference clock for the primary PLL
FINDIV[6:0]	Input	Input clock divider for PLL1 and PLL2
FBDIV[6:0]	Input	Sets the divider value for the PLL1 and PLL2 feedback.
OADIV[4:0]	Input	Multiplier value for PLL1 and PLL2, corresponding to CLK_OUT1 and CLK_OUT4
OBDIV[4:0]	Input	Multiplier value for PLL1 and PLL2, corresponding to CLK_OUT2 and CLK_OUT5
OCDIV[4:0]	Input	Multiplier value for PLL1 and PLL2, corresponding to CLK_OUT3 and CLK_OUT6
OAMUX[2:0]	Input	Phase shift value for PLL1 and PLL2, corresponding to CLK_OUT1 and CLK_OUT4
OBMUX[2:0]	Input	Phase shift value for PLL1 and PLL2, corresponding to CLK_OUT2 and CLK_OUT5
OCMUX[2:0]	Input	Phase Shift value for PLL1 and PLL2, corresponding to CLK_OUT3 and CLK_OUT6
CLK_OUT1	Output	Output clock 1
CLK_OUT2	Output	Output clock 2
CLK_OUT3	Output	Output clock 3
CLK_OUT4	Output	Output clock 4
CLK_OUT5	Output	Output clock 5
CLK_OUT6	Output	Output clock 6
LOCK	Output	Active high signal indicating that steady-state lock has been achieved between the reference clock and the PLL feedback signal.

Table 3 describes the configuration register bit details for dynamic mode configuration.

Table 3 • Configuration Register Description

Config. Bits	Signal	Name	Description
0	DYNCSEL	Clock input C dynamic select	Configures clock input C to be sent to GLC for dynamic control.
1	DYNBSEL	Clock input B dynamic select	Configures clock input B to be sent to GLB for dynamic control.
2	DYNASEL	Clock input A dynamic select	Configures clock input A for dynamic control.
<5:3>	VCOSEL[2:0]	VCO gear control	Three-bit VCO gear control for four frequency ranges
6	STATCSEL	MUX select on input C	MUX selection for clock input C
7	STATBSEL	MUX select on input B	MUX selection for clock input B
8	STATASEL	MUX select on input A	MUX selection for clock input A
<13:9>	DLYC[4:0]	YC output delay	Sets the output delay value for YC.
<18:14>	DLYB[4:0]	YB output delay	Sets the output delay value for YB.
<23:19>	DLYGLC[4:0]	GLC output delay	Sets the output delay value for GLC.
<28:24>	DLYGLB[4:0]	GLB output delay	Sets the output delay value for GLB.
<33:29>	DLYGLA[4:0]	GLA output delay	Primary, GLA output delay
34	XDLYSEL	System delay select	When selected, inserts system delay in the feedback path
<39:35>	FBDLY[4:0]	Feedback delay	Sets the feedback delay value for the feedback element.
<41:40>	FBSEL[1:0]	Primary feedback delay select	Controls the feedback MUX: no delay, include programmable delay element, or use external feedback.
<44:42>	OAMUX[2:0]	Secondary 2 output select	Selects from the VCO's four phase outputs for GLC/YC.
<47:45>	OBMUX[2:0]	Secondary 1 output select	Selects from the VCO's four phase outputs for GLB/YB.
<50:48>	OCMUX[2:0]	GLA output select	Selects from the VCO's four phase outputs for GLA.
<55:51>	OCDIV[4:0]	Secondary 2 output divider	Sets the divider value for the GLC/YC outputs.
<60:56>	OCBDIV[4:0]	Secondary 1 output divider	Sets the divider value for the GLC/YC outputs.
<65:61>	OADIV[4:0]	Primary output divider	Sets the divider value for the GLA.
<72:66>	FBDIV[6:0]	Feedback divider	Sets the divider value for the PLL core feedback.
<79:73>	FINDIV[6:0]	Input divider	Input clock divider (/n). Sets the divider value for the input delay on CLKA.

For detailed description of the multiplier, divisor, phase shift, and delay bus, refer to the PLL details in the *IGLOO FPGA Fabric User's Guide*, available at www.actel.com/documents/IGLOO_UG.pdf.

Utilization Details

This design was verified in the IGLOOe AGLE600V2-484FBGA device, but is applicable to all IGLOO and ProASIC3 devices with the minimum resource requirement. [Table 4](#) lists the utilization results for the targeted device.

Table 4 • Logic Utilization

Resource	Used/Total	Percentage (%)
Core	352 / 13824	2.55
IO (with clocks)	49 / 270	18.15
GLOBAL (chip + quadrant)	8 / 18	44.44
PLL	2 / 6	33.33

Simulation

Verification of the core is done by simulation in ModelSim®. The testbench generates the necessary inputs for the IP. The simulation was performed for the best case, typical, and the worst case delays, and gave satisfactory results. [Figure 2 on page 7](#) and [Figure 3](#) show the simulation results for static and dynamic modes.

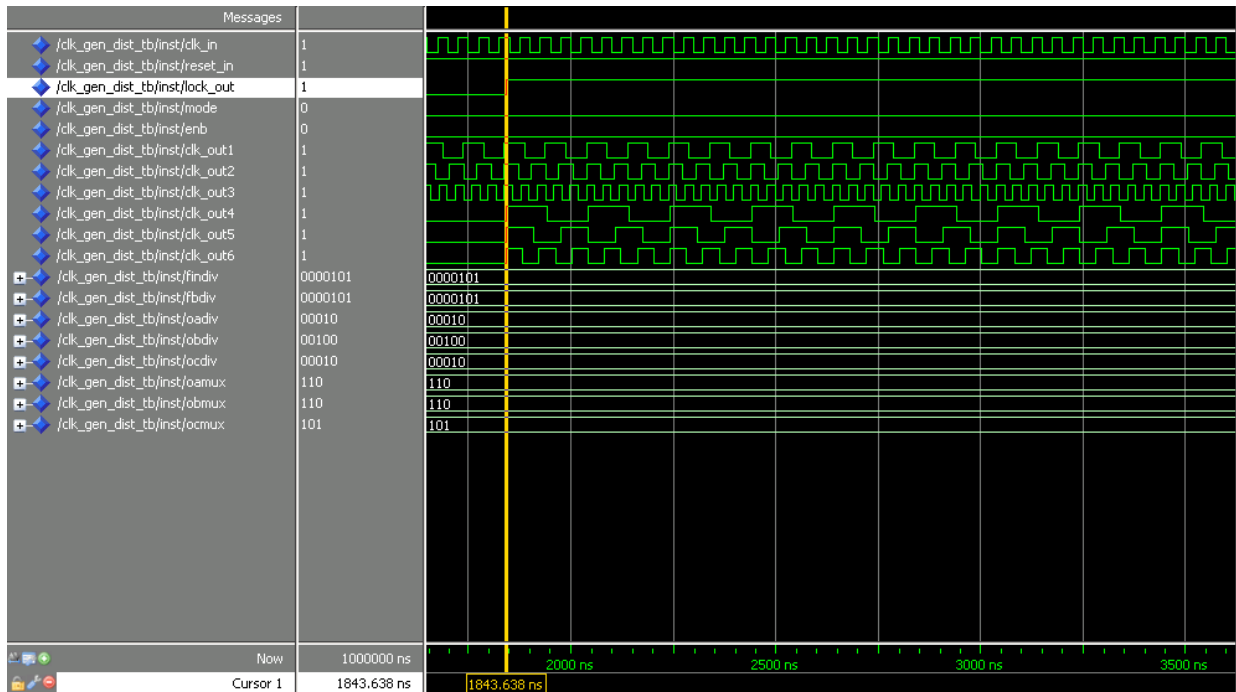


Figure 2 • Simulation Results – Static Mode

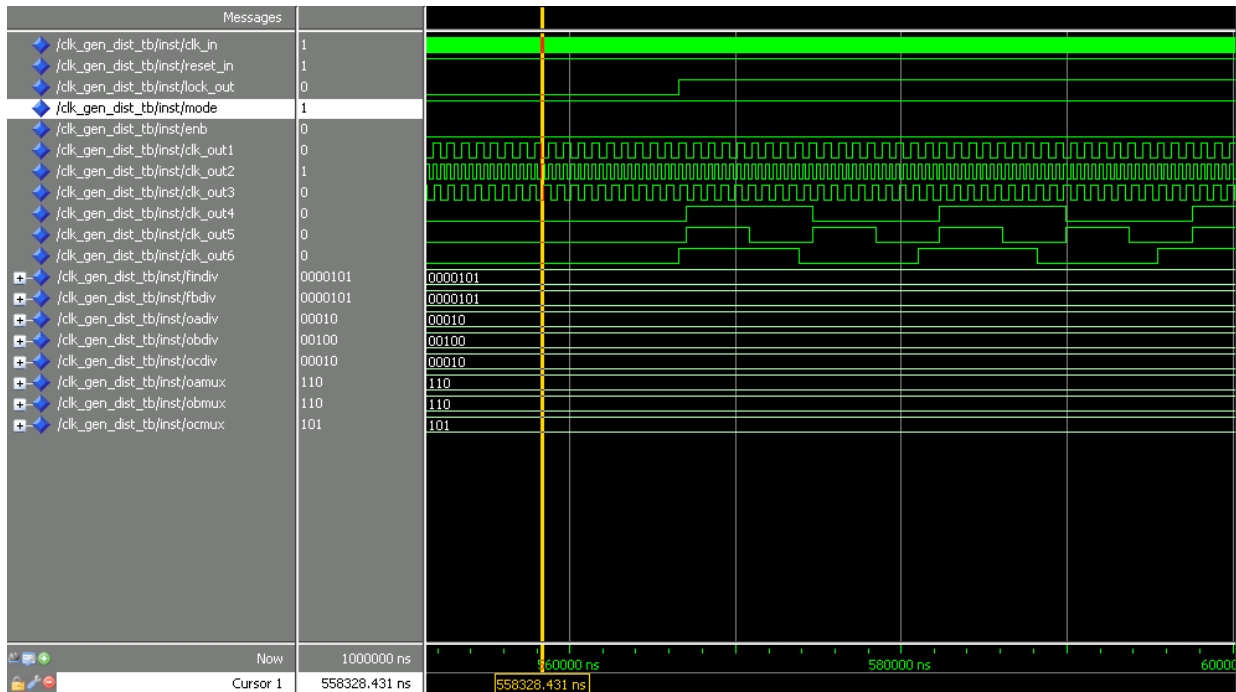


Figure 3 • Simulation Results – Dynamic Mode

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