

Metastability Characterization Report for Microsemi Antifuse FPGAs

Introduction

Whenever asynchronous data is registered by a clocked flip-flop, there is a probability of setup or hold time violation on that flip-flop. In applications such as synchronization or data recovery, due to the asynchronous nature of the data input to the flip-flops, the data transition time is unpredictable with respect to the active edge of the clock. The susceptibility of a circuit to reach this metastable state can be described using a probabilistic equation. Setup or hold violations cause the output of the flip-flop to enter a symmetrically balanced transient state, called a metastable state. The metastable state is manifested in a bistable device by the outputs glitching, going into an undefined state somewhere between a "1" and "0," oscillating, or by the output transition being delayed for an indeterminable time. Once the flip-flop has entered the metastable state, the probability that it will still be metastable later has been shown to be an exponentially decreasing function of time. Because of this property, a designer should simply wait for additional time after the specified propagation delay before sampling the flip-flop output so that the designer can be assured that the likelihood of metastable failure is remote enough to be tolerable. The additional time of waiting becomes shorter, even though still more than zero, as the technology improves and semiconductor devices reach higher ranges of speed.

This document discusses a description of metastability equations followed by metastability characterization of Microsemi antifuse FPGAs. This application note also provides examples on the usage of metastability equations.

Theory of Metastability

In general, the mean time between failures (MTBF) should be defined statically. [Figure 1 on page 2](#) depicts a simple circuit, used to synchronize an asynchronous data with the system clock. [EQ 1](#) shows the relation between MTBF and the clock-to-out settling time of a flip-flop:

$$\text{MTBF} = (e^{(T_s / \tau)}) / (T_0 * f_d * f_c) \quad \text{EQ 1}$$

$$T_s = T_{co} + T_{met} \quad \text{EQ 2}$$

In [EQ 1](#) and [EQ 2](#):

- T_s = Total flip-flop output settling time.
- T_{co} = Flip-flop clock-to-out delay.
- T_{met} = Additional settling time added to the normal clock-to-out delay of the flip-flop before sampling the output of the flip-flop.
- t = Metastable decay constant.
- T_0 = Metastability aperture at $T_{co} = 0$ ns (This parameter represents the likelihood that a flip-flop will enter a metastable state).
- f_d = Data transition rate (Twice the data frequency for periodic signals since there are two transitions per one period).
- f_c = Clock frequency

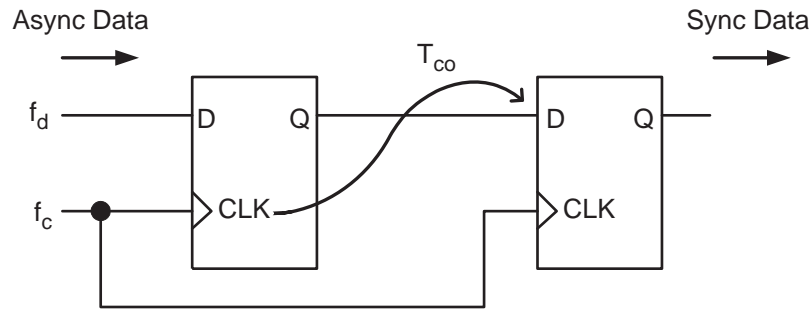


Figure 1 • Example of Synchronization Circuit

As mentioned earlier, the aperture represents the likelihood of the flip-flop to enter a metastable state. The aperture is defined as a time window within the clock period. Data transitioning inside the aperture will cause the flip-flop output settling time to be greater than $T_{co} + T_{met}$. The aperture is calculated by recording the number of instances in which the settling time exceeds the specified $T_{co} + T_{met}$. The metastability aperture decreases exponentially as the allowed settling time ($T_{co} + T_{met}$) increases:

$$\text{Aperture} = T_0 * (e^{-(T_{co} + T_{met})/\tau})$$

EQ 3

If the data transition occurs within the aperture, the flip-flop will stay metastable beyond the allocated settling time ($T_{co} + T_{met}$); and therefore, the second flip-flop would register invalid data (Figure 1). The probability of an asynchronous data transition is uniformly distributed over the clock period. Therefore, the probability of a single data transition occurring in the metastable aperture is calculated by the following:

$$p = \text{aperture} / T_c$$

EQ 4

Where T_c is the clock period.

In each clock cycle, the failure occurs if the data transition time is within the aperture. Therefore, the number of failures in one clock cycle can be derived by the following:

$$n_e = n * p = n * (\text{aperture} / T_c)$$

EQ 5

Where n_e represents the number of errors per clock cycle, and n is the number of data transitions per clock period (f_d / f_c).

The number of clock cycles in the operation time (N) is the total time divided by the clock period or

$$N = T_{\text{operation}} / T_c$$

EQ 6

Combining EQ 5 and EQ 6 results in the total number of failures per operation time (N_e):

$$N_e = N * n_e = (T_{\text{operation}} / T_c) * [(f_d / f_c) * (\text{aperture} / T_c)]$$

EQ 7

Since $T_c = 1 / f_c$, EQ 7 can be simplified to:

$$N_e = T_{\text{operation}} * f_d * f_c * \text{aperture}$$

EQ 8

MTBF is defined as the operation time divided by the number of failures or:

$$\text{MTBF} = 1 / (f_d * f_c * \text{aperture}) = 1 / (T_0 * e^{-(T_{co} + T_{met})/\tau} * f_d * f_c)$$

EQ 9

FPGA Metastability Characterization

Like other FPGA manufacturers, in order to absorb the fixed value of the $e^{T_{co}}$ term, Microsemi simplifies EQ 9 to the following form:

$$MTBF = e^{C2 * T_{met}} / (C1 * f_d * f_c)$$

EQ 10

Where C2 is a constant inversely proportional to the metastability decay constant, and C1 is the proportionality constant that is similar to aperture.

The FPGA metastability characterization is a series of tests that are conducted in order to identify the value of C1 and C2. There are several environmental and test condition factors that influence the characterization. These factors include but are not limited to the rise time of data and clock signals, input voltage levels and operating voltage and temperature. Moreover, increased system noise due to switching of both internal nodes and I/Os can influence the metastability results. Therefore, it is essential to provide a suitable environment for testing.

Test Design Description

Figure 2 shows a schematic of the test circuit used to characterize the metastability in Microsemi devices. The propagation delay, operating under specified setup and hold time, is measured from the output of flip-flop DFF#1 to the input of flip-flop DFF#3. This value is denoted by:

$$T_{min} = T_{cof}(DFF\#1) + T_{delay} + T_{su}(DFF\#3)$$

EQ 11

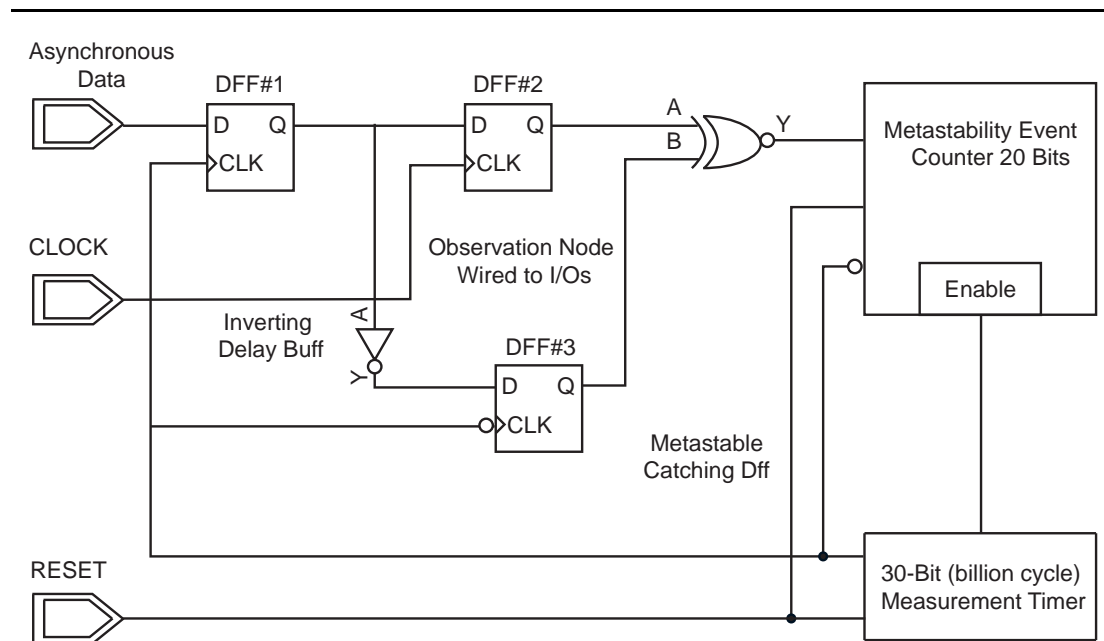


Figure 2 • Test Circuit

Where T_{delay} is the propagation delay from output of DFF#1 to input of DFF#3, T_{cof} is the clock-to-out delay of DFF#3 and T_{su} represents the setup time requirement of DFF#3. T_{min} corresponds to the T_{co} in EQ 9 on page 2 and is the reference time to which the additional settling time, T_{met} , is added for characterization of metastability.

DFF#2 is clocked on the same edge as DFF#1. Conversely, DFF#3 must resolve the signal driven from the metastable DFF#1 before the falling clock edge. As it can be seen in the design in Figure 2 on page 3, $T_{min} + T_{met}$ is the difference between the rising and falling edge of the clock. Therefore, it can be easily set or measured by adjusting the duty cycle of clock signal. A detectable metastable event occurs when

DFF#2 and DFF#3 are in the SAME state. In the expected operation, DFF#2 and DFF#3 are in opposite states due to the inverter in the DFF#3 input data path. The XNOR gate allows the event counter to record these metastable events. After a billion clock cycles, the counter is read and the MTBF is calculated.

In this test, T_{\min} was resolved to within $\pm 0.01\%$ of the duty cycle at 10 MHz. This translates to an error of ± 10 ps.

The other test setup parameters are as follows:

- Clock and data inputs are driven from independent pulse generators (<1 nS Rise time)
- For SX, RTSX32, ACT1, ACT2, ACT3, and MX the clock input levels are from 0 V to 2.5 V. These levels were required due to impedance matching requirements of our test fixture. Data input is driven 0V to 3.3 V.
- For RTSX72S, A54SX72A, RT54SX32S, A54SX32A, and AX1000, the clock input levels are from 0 V to 1.5 V. Data input is driven 0 V to 1.65 V.
- Power supply settings were as follows:
 - AX1000: VCCR, VCCI, VPP = 3.3 V; VCCA = 1.5 V; VKS = 0 V
 - RT54SX72S, A54SX72A, RT54SX32S, A54SX32A: VCCI = 3.3 V; VCCA, VSV, VPP = 2.5 V; VKS = 0V
 - SX, RT54SX32: VCCA, VCCI = 3.3 V, VCCR = 5.0 V
 - ACT1: VCC, VSV, VPP = 5.0; VKS = 0 V
 - ACT2: VCC, VSV, VPP = 5.0; VKS = 0 V
 - ACT3: VCC, VSV, VPP = 5.0; VKS = 0 V

Metastability Measurement Results

EQ 10 can be reformulated into the following:

$$\ln(\text{MTBF}) = C_2 * T_{\text{met}} - \ln(C_1 * f_d * f_c)$$

EQ 12

The plot of EQ 12 is a linear relationship between $\ln(\text{MTBF})$ and T_{met} where C_2 is the slope of the line. Figure 3 and Figure 4 on page 5 show the plot of EQ 12 for Microsemi antifuse FPGA families. C_1 and C_2 can be calculated from any two data points.

The metastability theory indicates that C_1 and C_2 are independent of the test clock and data frequency. The test results concur within experimental tolerances. The calculation of C_1 and C_2 are given in Table 1 on page 6. The plots of MTBF for the SX, RTSX, MX, ACT1, and XL products include a plot for the ACT3 product as a reference. For example, SX (0.35 μm) demonstrates good improvement over ACT3. On the other hand, RT54SX32 and A42MX16 are similar to ACT3 in metastability performance.

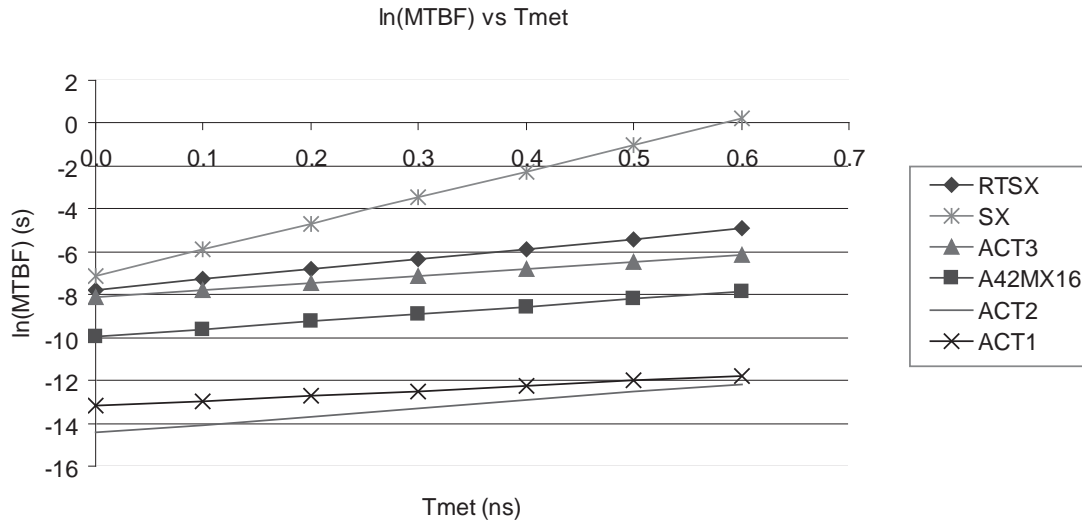


Figure 3 • Metastability Comparison of Microsemi FPGA Families

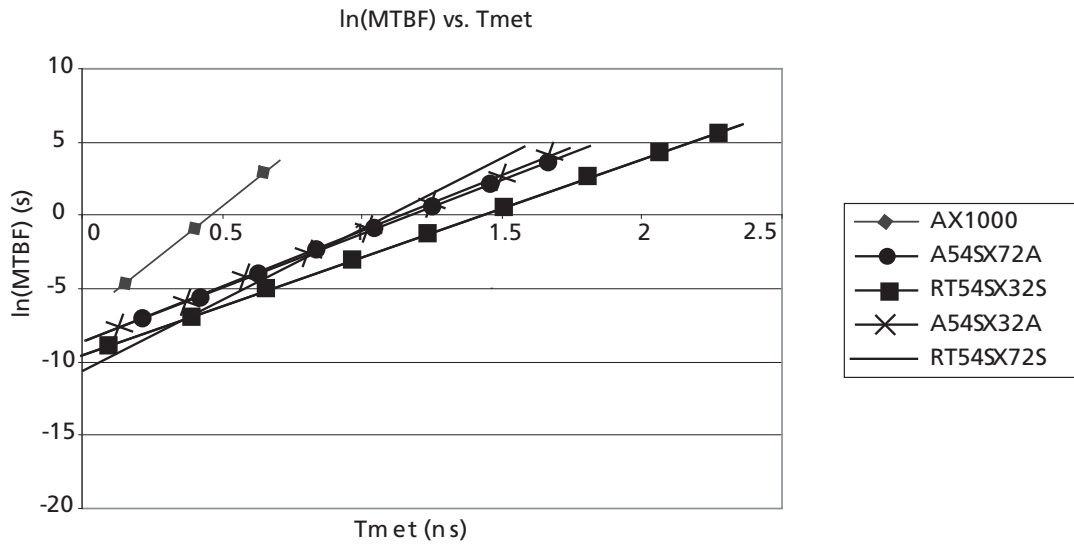


Figure 4 • Metastability Comparisons of SX-A/RTSX-S/Accelerator® Families

Table 1 • Metastability Coefficients for Microsemi FPGA Families

f_c = 10MHz		
Device Family	C1 (s)	C2 (1/s)
RTAX-S/SL/DSP (0.15 μm)	1.0196E-10	1.8222E10
AX1000 (0.15 μm)	1.857E-11	1.539E10
RTSX32SU (0.25 μm)	3.325E-10	7.157E9
A54SX32A (0.25 μm)	1.005E-10	7.618E9
RTSX72SU (0.25 μm)	7.12E-10	9.766E9
A54SX72A (0.22/0.25 μm)	9.26E-11	7.391E9
RT54SX32 (0.35 μm)	2.021E-11	1.2157E+10
RT54SX32 (0.6 μm)	3.933E-11	4.7342E+09
1460A(ACT3) (0.8 μm)	5.570E-11	3.2700E+09
MX16 (0.45 μm)	3.464E-10	3.4704E+09
1240XL(ACT2) (0.6 μm)	3.16E-08	3.83E+09
1020A(ACT1) (1.0 μm)	8.93E-09	2.35E+09

Examples of Metastability Coefficients Usage

Metastability shows a statistical nature and designers should allow enough additional time (T_{met}), so that the likelihood of metastable failure is remote enough to be tolerable by the design specification.

For example, consider that the simple circuit in [Figure 1 on page 2](#) is implemented in a A54SX32A device in order to synchronize an asynchronous data input to the FPGA. The following parameters are given to designer by either design specification or post-layout timing analysis:

T_{co} = 10 ns corresponding to a clock frequency of 100 MHz.

Asynchronous data transition rate = 12.5 MHz

Tolerable MTBF = 20 years

If designer does not allow additional sampling time ($T_{met} = 0$ ns) and run the clock at the rate of 100 MHz, [EQ 12 on page 4](#) will result in MTBF = 7.96 μs. This means that a metastability error will occur at the output of the second flip-flop at every 7.96 μs. This value exceeds the required MTBF of 20 years indicated in the design specification. In order to meet this requirement, the designer must allow additional T_{met} in the sampling time, which can be calculated as follows:

20 years = 20 * 365 * 24 * 3600 = 630,720,000 seconds

$\ln(630,720,000) = 7.618E+09 * T_{met} - \ln(1.005E-10 * 100E6 * 12.5E6) \geq T_{met} = 4.20$ ns

Therefore, an additional 4.20 ns sampling time will fulfill the required MTBF.

List of Changes

Revision*	Changes	Page
Revision 4 (March 2012)	Metastability coefficients were added to Table 1 • Metastability Coefficients for Microsemi FPGA Families for the RTAX-S/SL/DSP family. The device family name RT54SX32S was corrected to RTSX32SU; the device family name RT54SX72S was corrected to RTSX72SU (SAR 22143).	6
Revision 3 (October 2007)	In the " Examples of Metastability Coefficients Usage " section, the metastability error at the second flip-flop was changed from 51.2 μ s to 7.96 μ s.	6
Revision 2 (May 2004)	This document was updated to provide a detailed descriptions of the calculations being made.	N/A
Revision 1 (March 2004)	Table 1 • Metastability Coefficients for Microsemi FPGA Families was updated.	6
	Figure 4 • Metastability Comparisons of SX-A/RTSX-S/Axcelerator® Families is new.	5

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*



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