
Using ProASIC^{PLUS} Clock Conditioning Circuits

Introduction

ProASIC^{PLUS} devices include two clock conditioning circuits on opposite sides of the die. Each clock conditioning circuit contains a Phase Locked Loop (PLL), several delay lines, clock multipliers/dividers, and all the circuitry for interconnection of the external bidirectional global pads and Low-Voltage Positive Emitter Coupled Logic (LVPECL) pads to the global low-skew network. The circuitry offers the flexibility to bypass the PLL core using just the surrounding dividers and delay elements.

The clock conditioning circuit enables you to perform the following functions:

- Clock phase adjustment using the PLL's multi-phase Voltage Controlled Oscillator (VCO)
- Clock delay minimization using the various delay elements inserted in different paths
- Clock frequency synthesis using the different dividers around the PLL
- Any combination of the above

ProASIC^{PLUS} PLLs can be configured either statically or dynamically. For a PLL static configuration, you can invoke SmartGen to set the various parameters. In dynamic mode, designers are able to set all the configuration parameters using either the external JTAG port or an internally-defined serial interface. The dynamic-mode PLL can be switched to static mode during operation by just changing a mode selection bit. You can have a single, stable static configuration or can switch to dynamic mode and run the clock at a different speed for a selected sequence of events. Repeating the whole design flow—from rewriting the HDL code to programming the device with the new configuration—is not necessary. This feature also enables you to compensate for temperature drift or other external changes.

ProASIC^{PLUS} PLL Core Characteristics

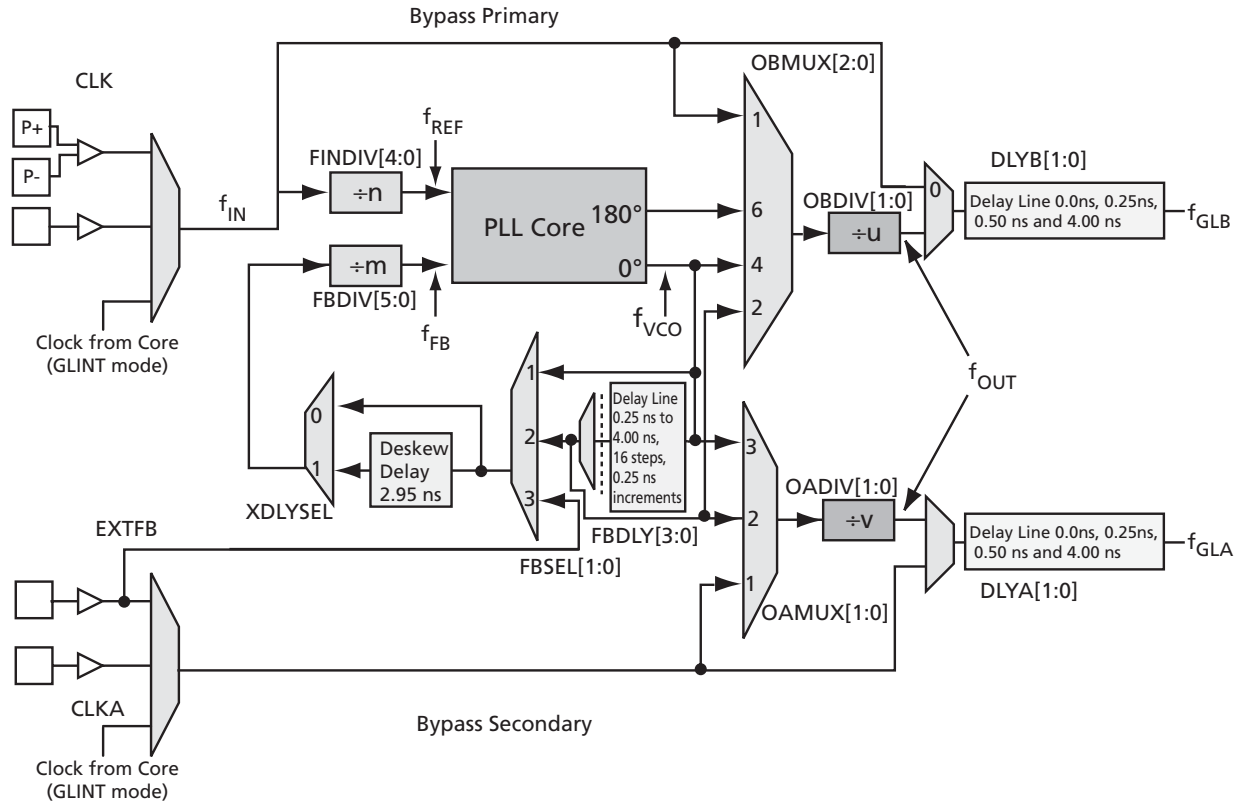
For further details and characterized timing numbers, please refer to the *ProASIC^{PLUS} Flash Family FPGAs* datasheet.

Clock Conditioning Circuit Features

This section introduces various features of the clock conditioning block, discusses the various use models, and briefly describes the interface to the various external pads.

Architecture

Figure 1 and Table 1 on page 3 show the internal architecture of the ProASIC^{PLUS} clock conditioning circuitry. Refer to the following sections for details about the use of the different elements of the block diagram.



Notes:

1. FBDLY is a four-bit programmable delay line from 0 to 4 ns in 250 ps increments.
2. DLYA, DLYB, DLYAFB are two-bit programmable delay lines with values 0, 250 ps, 500 ps, and 4 ns.
3. OBDIV will also divide the phase-shift since it takes place after the PLL Core.

Figure 1 • Internal Architecture of the ProASIC^{PLUS} Clock Conditioning Circuitry

Table 1 • Clock Conditioning Circuitry Multiplexor (MUX) Settings

	Feedback Path: Negative Delay to the PLL Output Signal	Comments	
XDLYSEL			
0	+0	Use feedback as is	
1	-2.95 ns	Deskew feedback by advancing clock by system delay	
FBSEL			
1	+0	Internal feedback	
2	-0.25 up to -4 ns	Internal feedback and advance clock in 0.25 ns increments up to 4 ns (FBDLY)	
3	EXTFB	Use external feedback	
OBMUX			
0	Bypass, no divider	OAMUX	GLA
1	Bypass, use divider	0	Bypass, no divider
2	Delay clock in 0.25ns increments up to 4 ns (FBDLY)	1	Bypass, use divider
4	+0°	2	Delay clock in 0.25 ns increments up to 4 ns (FBDLY)
5	Not Used	3	+0°
6	+180°		
7	Not Used		
DLYB		DLYA	
0	+0	0	+0
1	+0.25 ns	1	+0.25 ns
2	+0.50 ns	2	+0.50 ns
3	+4.0 ns	3	+4.0 ns

Interface and Access to the Global Network

The clock conditioning block enables the connection from the ProASIC^{PLUS} bidirectional global pads, the differential LVPECL input pad pair, user I/Os, or even an internally generated signal to the global low-skew network and/or the PLL reference clock. The circuitry offers the possibility of driving the global networks with the outputs from the PLL core. The two-per-side global pads connect to the global networks or PLL reference clock input on the same side. For example, one global clock network can be driven directly from the output clock of the PLL, whereas the other global clock network can be driven from the same output clock but with phase-shift or time delay.

Physical Implementation

Each side of the chip contains a clock conditioning circuit based upon a 180 MHz PLL block (Figure 1 on page 2).

Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads. The global lines may be driven by the LVPECL global input pad, the outputs from the PLL block, or both. Each global line can be driven by a different output from the PLL. Unused global pins can be configured as regular I/Os or left unconnected. They default to an input with pull-up. The two signals available to drive the global networks have the following options (Figure 2 on page 5):

Global A (Secondary Clock)

- Output from Global MUX A
- Conditioned version of PLL output (f_{OUT}) – delayed or advanced
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)¹

Global B

- Output from Global MUX B
- Delayed or advanced version of f_{OUT}
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)¹

Functional Description

Each PLL block contains four programmable dividers as shown in [Figure 1 on page 2](#). These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 32.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 180 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by [EQ 1](#) (f_{IN} is the input clock frequency):

$$f_{VCO} = f_{IN} * m/n \quad \text{EQ 1}$$

- The third and fourth dividers (u and v) permit each of the signals applied to the global network to be further divided by integer factors ranging from 1 to 4.

[EQ 2](#) and [EQ 3](#) enable you to define a wide range of frequency multipliers and divisors.

$$f_{GLB} = f_{IN} * m / (n * u) \quad \text{EQ 2}$$

$$f_{GLA} = f_{IN} * m / (n * v) \quad \text{EQ 3}$$

The clock conditioning circuit can advance or delay the clock up to 8 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0° and 180°. Prior to the application of signals to the global drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input setup times or other applications. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This prevents unnecessary and unwieldy design and software work.

[Figure 2 on page 5](#) shows the clock inputs (excluding the external feedback input) to the PLL core. CLK is the primary input clock, while CLKA, the second input clock, is used as a reference clock for the secondary output clock (GLA) of the PLL core when the PLL is bypassed. The CLKA input clock is used only when the PLL is in bypass secondary mode. This is discussed in more detail in the [“Bypass Modes” section on page 7](#).

1. This mode is available through the delay feature of the Global MUX driver.

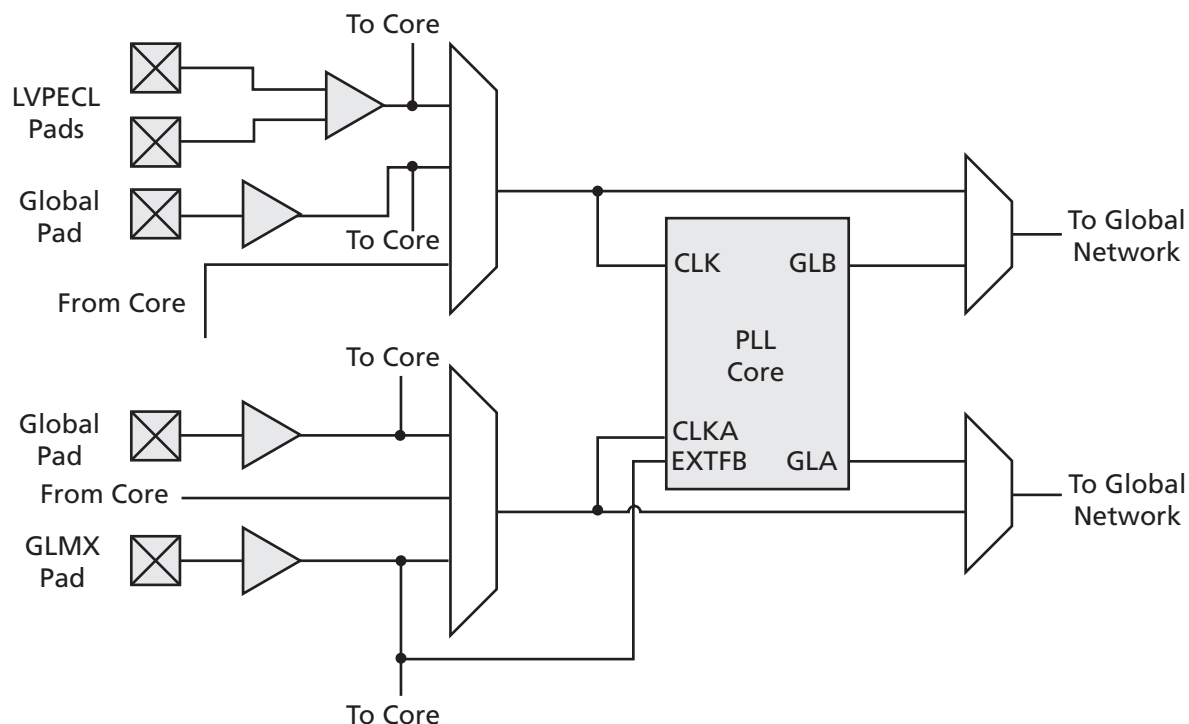


Figure 2 • External and Internal Interface to the ProASIC^{PLUS} Clock Conditioning Circuitry

Configurability

The clocking circuitry is fully reconfigurable using either Flash configuration bits (set in the programming bitstream) or a simple asynchronous interface (dynamically accessible from internal user registers or the JTAG interface). This allows parameters such as the PLL divide ratios to be modified during operation.

For more information on the dynamic reconfiguration of the PLLs, refer to the [ProASIC^{PLUS} PLL Dynamic Reconfiguration Using JTAG](#) application note.

Detailed Application Information

Clock Division and Multiplication

In addition to the PLL, the block contains four programmable dividers, as shown in [Figure 3 on page 6](#).

The first divider, " $\div n$," is located in the input path to provide integer division factors ranging from 1 up to and including 32.

Two other dividers, " $\div u$ " and " $\div v$," are located in the paths of the two PLL output clocks, CLKA and CLKB. They enable further division of these outputs by factors of 1, 2, 3, and 4.

As a consequence, the primary output clock frequency is given by [EQ 4](#). The output " $\div u$ " and " $\div v$ " dividers are not phase synchronized with the input clock or with each other.:

$$\text{CLKB} = \text{CLKOUTPLL} \div u$$

EQ 4

and the secondary output clock frequency is given by [EQ 5](#):

$$\text{CLKA} = \text{CLKOUTPLL} \div v$$

EQ 5

In other words, the CLKB and CLKA frequencies are related according to EQ 6:

$$\text{CLKB} = (v \times \text{CLKA}) \div u \tag{EQ 6}$$

Overall, you are able to define a wide range of multiplication and division factors. CLKB's frequency can be derived from the CLK frequency using EQ 7 and EQ 8:

$$\text{CLKB} = [m \div (n \times u)] \tag{EQ 7}$$

$$\text{CLKA} = [m \div (n \times v)] \tag{EQ 8}$$

It is well known that arbitrary values of CLKA and CLKB cannot be synthesized for a given value of CLK. EQ 6, EQ 7, and EQ 8 allow you to check all the possible combinations of CLKA and CLKB frequencies. When calculating the desired value of " $\div m$ " and " $\div n$," consider the frequency range constraints. The output dividers ($\div u$ and $\div v$) were not designed with a reset signal, so there is no way to guarantee synchronization with the input clock and with each other. The phase coming into the output dividers will be aligned with the input clock, but the phase coming out of the divider will be unpredictable. If the PLL has been configured such that the output dividers are greater than one, the corresponding clock output (GLB or GLA) may have an indeterminate phase shift with respect to the clock and with each other.

The output delay (DLYB, DLYA) will still be correct, but since the phase coming into the delay module is unpredictable, the clock output may yield unexpected results.

Since ModelSim cannot generate an accurate simulation based upon unpredictability, a 180° phase shift may be seen on the clock output when its output divider is not equal to one.

If having an output divider greater than one is unavoidable, the internal PLL output divider has to be replaced with your own clock divider.

Clock Delay

The clock conditioning block also performs positive and negative clock delay operations. Delay elements are placed in the output clock paths as well as in the feedback path. They enable up to 8 ns delay with increments of 250 ps. As shown in Figure 3 and Figure 4, these delays can be positive or negative. Using a delay element in the output clock path results in a positive output clock delay relative to the input reference clock. Positive delay in the feedback path is equivalent to negative delay of the output clock; that is, advancing the output clock relative to the input reference clock. This feature enables you to remove the delay due to the input clock pad to meet setup time requirements, or to delay the clock to meet the clock-to-out timing requirements.

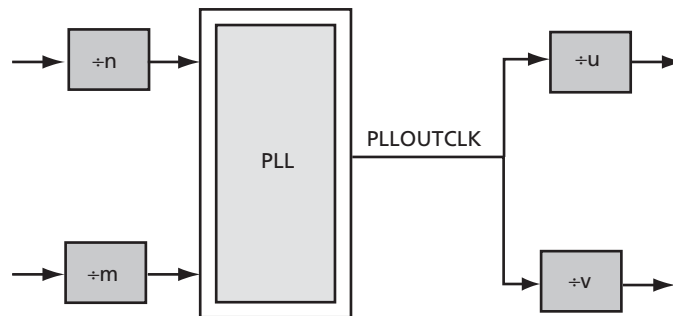


Figure 3 • Simplified Clock Conditioning Block Diagram Showing Multiplication and Division

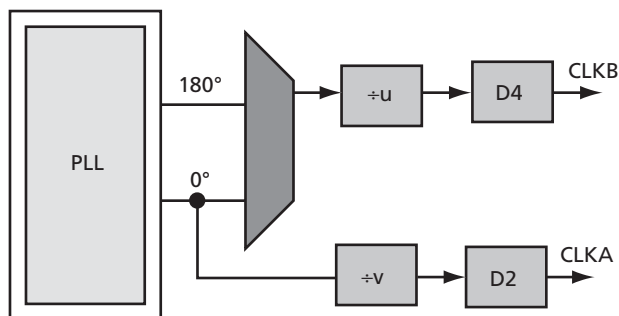


Figure 4 • Phase Shift of Primary Clock

Phase Shift

The PLL core allows you to select one of two clock phases of the primary clock CLKB – 0 and 180 degrees. As shown in [Figure 4](#), the secondary clock, CLKA, cannot be phase-shifted and is tied to the 0° output phase of the PLL. The setting of the multiplexer selection lines is performed by the software and is transparent to you. If phase synchronization between CLKA and CLKB is required, Actel recommends that the PLL's output divider be replaced by a user created clock divider. Refer to the "[Clock Division and Multiplication](#)" section on [page 5](#) for details.

Bypass Modes

The clock conditioning circuit allows CLKA, CLKB, or both to bypass the PLL core. This section describes methods of bypassing the PLL core and various possibilities for configuring the output clock even when the PLL is bypassed. The bypass modes are extremely useful for optimizing the global network resources. For more information on global network resources, refer to the "[Optimal Usage of the Global Resources and PLL](#)" section on [page 14](#).

As depicted in [Figure 5](#), both input clocks can be independently divided, delayed, or simultaneously divided and delayed without going through the PLL core. A path of the bypass mode of GLB is marked as "Bypass Primary" with a thick line. Notice that the "÷n" divider is also bypassed and the divider "÷u" can be used in combination with the delay element. Similarly, the bypass mode of GLA is shown as "Bypass Secondary" and the divider "÷v" can be used in combination with the delay element downstream. Additionally, the secondary output (GLA) can have its own incoming reference clock as depicted in [Figure 2](#) on [page 5](#).

If the PLL is in bypass mode, an internal signal is automatically set to switch off the PLL core to avoid unnecessary power dissipation. The place-and-route tool configures this signal using a Flash bit. Note that this signal can also be dynamically reconfigured.

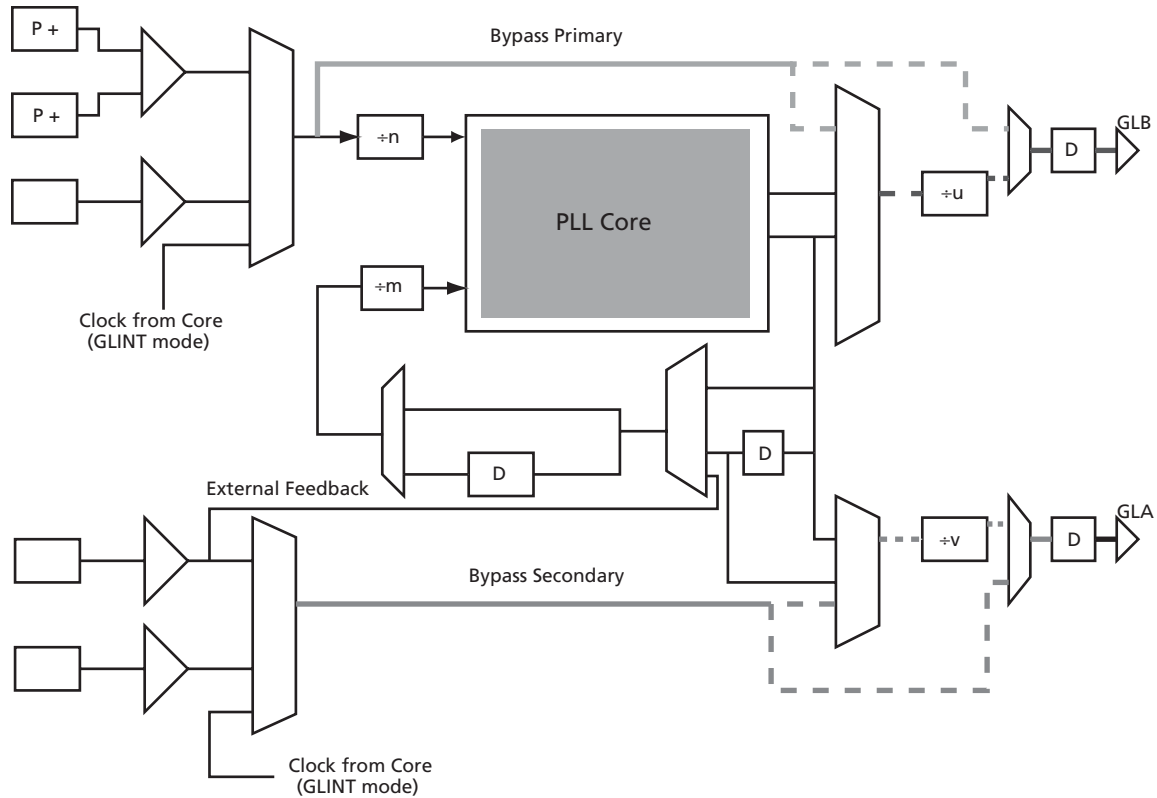


Figure 5 • Detailed Schematic Drawing of the Bypass Modes

Lock Function

A Lock signal is provided to indicate that the PLL has locked onto the incoming clock signal. You can employ the "Lock" signal as a soft reset of the logic driven by GLB and/or GLA.

Internal and External PLL Feedback

The clock conditioning circuitry enables the you to implement the feedback clock signal using an external clock or the output of the PLL itself, as illustrated in Figure 6.

In the case of external feedback, the GLMX pin of the device must be used as the input port of the feedback clock.

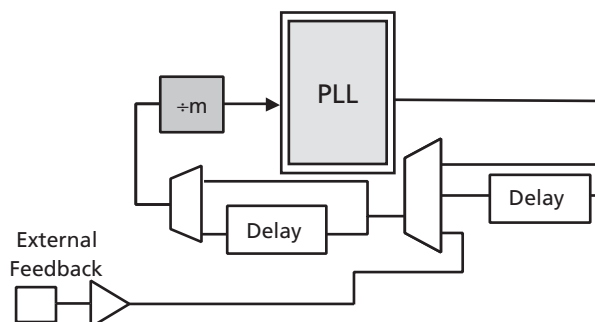


Figure 6 • Block Diagram of the Feedback Circuitry in an HDL Design

Integration of ProASIC^{PLUS} PLL in an HDL Design

The Primitive Port List

The following is a simplified Verilog description of the PLL primitive. It is intended to show the port list.

```

module PLLCORE (GLA, GLB, LOCK, SDOUT, CLK, CLKA, EXTFB, SCLK, SSHIFT, SDIN, SUPDATE,
MODE, FINDIV, FBDIV, OADIV, OBDIV, OAMUX, OBMUX, FBSEL, FBDLY, XLDYSEL, DLYA, DLYB,
STATASEL, STATBSEL);
input CLK, CLKA, EXTFB, SCLK, SSHIFT, SDIN, SUPDATE, MODE;
input [4:0] FINDIV;
input [5:0] FBDIV;
input [1:0] OBDIV;
input [1:0] OADIV;
input [1:0] OAMUX;
input [2:0] OBMUX;
input [1:0] FBSEL;
input [3:0] FBDLY;
input [1:0] DLYA;
input [1:0] DLYB;
input XLDYSEL;
input STATASEL;
input STATBSEL;
output GLA, GLB, LOCK, SDOUT;
endmodule

```

Table 2 provides a description of the PLL core output ports.

Table 2 • PLL Core Output Ports

Port	Description
GLB	Primary clock output
GLA	Secondary clock output
LOCK	PLL lock signal (when low, the PLL is not locked)

The input ports can be divided into the following categories:

- Input Clocks
 - CLK – Input clock for primary clock
 - CLKA – Input clock for secondary clock. As explained in the “ProASIC^{PLUS} PLL Core Characteristics” section on page 1 and illustrated in Figure 6 on page 9, this input clock is used only in bypass mode.
 - EXTFB – External Feedback. Connects the output of the external feedback PAD to this port
- Dividers
 - FINDIV [4:0] – Five-bit input divider. The range is from 1 (encoded as "00000") to 32 (encoded as "11111").
 - FBDIV [5:0] – Six-bit divider in the feedback path. It is actually a multiplier of the input frequency. The division values range from 1 (encoded as "000000") to 64 (encoded as "1111111").
 - OBDIV [1:0] – Two-bit divider in the primary clock (GLA) output path. The division values range from 1, (encoded as "00,") to 4.
 - OADIV [1:0] – Two-bit divider in the secondary clock (GLB) output path. The division values range from 1 to 4. OBDIV and OADIV were not designed with a reset signal, so there is no way to guarantee synchronization with the input clock and with each other. The phase coming into the output dividers will be correct, but the phase coming out of the divider will be unpredictable.
- Delays
 - DLYA[1:0] – Additional delay value for GLA output. "00" means no delay.
 - DLYB[1:0] – Additional delay value for GLB output. "00" means no delay.
 - FBDLY [3:0] – Feedback delay values. The feedback delay values can be selected in 250 ps steps. "0000" encodes 250 ps while "1111" means 4 ns.
 - DLYAFB[1:0] – Additional delay value for GLA output in the feedback path
- Global Network and Feedback Path Multiplexing

The setting of these select lines is performed by the software and is completely transparent to you. The descriptions provided in Table 3 to Table 5 on page 11 are provided for completeness only.

- Input Multiplexing
 - STATASEL and STATBSEL indicate the multiplexer selection for CLKA and CLK inputs of the PLL. Refer to Figure 2 on page 5.
- PLL Configuration Mode
 - MODE indicates dynamic or static mode of the PLL. If set to "0," the PLL configuration mode is static. A separate application note, *ProASIC^{PLUS} PLL Dynamic Reconfiguration Using JTAG*, describes dynamic configuration.

Table 3 • OBMUX [2:0] Global Multiplexing in GLB Path

Value	Description
000	Select Bypass B
001	Select Global MUXB out
010	Select output of Delay Line
011	Reserved
100	Select Phase 0 of VCO for primary output clock
101	Not Used
110	Select Phase 180 of VCO for primary output clock
111	Not Used

Table 4 • OAMUX [1:0] Global Multiplexing in GLA Path

Value	Description
00	Select Bypass A
01	Select Global MUX A out
10	Select Output of Delay Line
11	Select Phase 0 of VCO

Table 5 • FBSEL[1:0] Selection of the PLL Feedback Clock (illustrated in Figure 7)

Value	Description
00	Selects MUX input of 0. Used for standby mode in standby logic block
01	Selects output of the delay line in the internal feedback path
10	Selects phase 0 of VCO output and skips delay elements in the internal feedback path
11	Selects the external feedback that can be an internal net or an external input

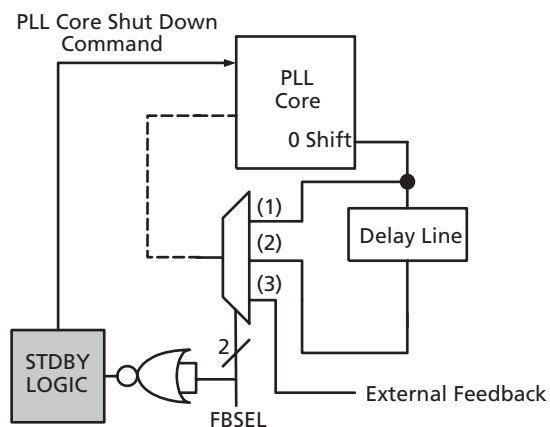


Figure 7 • Selection of the Feedback Loop by FBSEL [1:0]

PLL Generation

SmartGen, the Actel core generator, helps you set the PLL parameters or and generate HDL and EDIF description files. Figure 8 shows the main menu for PLL generation.

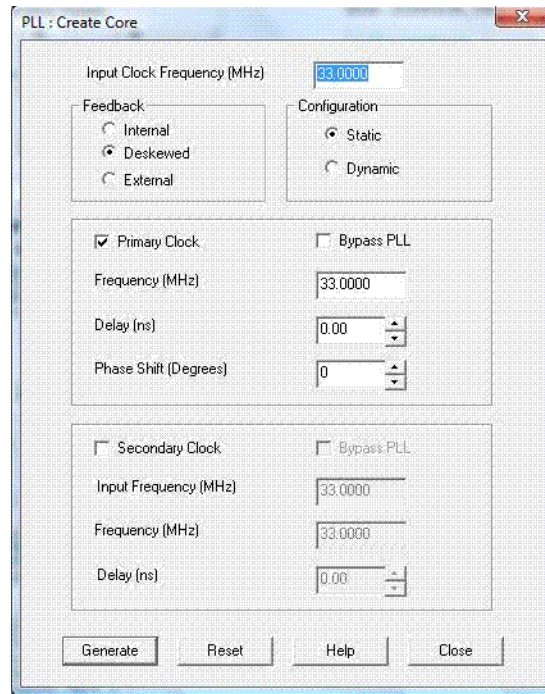


Figure 8 • SmartGen GUI for PLL Generation

The PLL generation tool offers different options that are described briefly in the following subsections. For more details, refer to the SmartGen online help.

The Input Clock Frequency must be within the 1.5 to 180 MHz range.

The Feedback section allows you to select between internal, deskewed, or external feedback. Selecting external feedback results in an additional input port to the PLL module which is driven by an external clock input. As mentioned earlier, the external clock feedback should be connected to the GLMX pin.

The Configuration section offers a selection between the static and dynamic configuration options. In dynamic mode, the configuration shift register ports and the MODE signal are accessible to the user's design. This allows switching between the Flash switch and shift register configuration.

For more information, refer to the [ProASIC^{PLUS} PLL Dynamic Reconfiguration Using JTAG](#) application note.

The Primary Clock section enables you to specify the output frequency, the delay, the phase shift (if any), and whether or not the PLL is bypassed.

The Secondary Clock sub-dialog box enables you to specify the output frequency, the delay (if any), and whether or not the PLL is bypassed. Notice that if the PLL is bypassed, you have the opportunity to specify a different input clock frequency for the secondary output clock.

The bottom of the main menu is a trace window where the tool provides useful information on the PLL generation. Read these messages carefully in case the expected combination of input and output frequencies is not generated.

For more information on the wide range of combinations, use the equations provided in the ["Clock Division and Multiplication"](#) section on page 5.

Main Menu of the PLL Generation Tool

After setting all the required parameters, you can generate one or more PLL configurations with HDL or EDIF descriptions by clicking the **Generate** button. SmartGen enables you to save the session results and messages in a "log" file.

A Verilog HDL description of a legal PLL core configuration and the surrounding circuitry is provided below. Notice that the file header provides a summary of all your parameter settings.

```

`timescale 1ns/10ps
// Name = MasterPLL
// configuration = static
// clocks = secondary
// feedback = external
// part family = APA
// input clock frequency = 50 MHz
// feedback select = 3
// feedback delay line = 2
// primary clock frequency = 60 MHz
// primary clock delay = 0.5 ns
// primary clock phase shift = 180 degrees
// input clock divider = 5
// feedback divider = 12
// feedback select = 3
// primary clock divider = 2
// primary clock select = 6
// primary clock delay line = 2
// secondary clock frequency = 120 MHz
// secondary clock delay = 0.75 ns
// secondary clock divider = 1
// secondary clock select = 2
// secondary clock delay line = 0
module MasterPLL (GLB, GLA, EXTFB, LOCK, CLK);
output GLB;
output GLA;
input EXTFB;
output LOCK;
input CLK;
PLLCORE U0(.GLA(GLA), .GLB(GLB), .LOCK(LOCK), .SDOUT(n1), .CLK(CLK), .CLKA(VSS),
.EXTFB(EXTFB), .SCLK(VSS), .SSHIFT(VSS), .SDIN(VSS), .SUPDATE(VSS), .MODE(VSS),
.FINDIV4(VSS), .FINDIV3(VSS), .FINDIV2(VDD), .FINDIV1(VSS), .FINDIV0(VSS),
.FBDIV5(VSS), .FBDIV4(VSS), .FBDIV3(VDD), .FBDIV2(VSS), .FBDIV1(VDD), .FBDIV0(VDD),
.OADIV1(VSS), .OADIV0(VSS), .OBDIV1(VSS), .OBDIV0(VDD), .OAMUX1(VDD), .OAMUX0(VSS),
.OBMUX2(VDD), .OBMUX1(VDD), .OBMUX0(VSS), .FBSEL1(VDD), .FBSEL0(VDD), .FBDLY3(VSS),
.FBDLY2(VSS), .FBDLY1(VDD), .FBDLY0(VSS), .XDLYSEL(VSS), .DLYA1(VSS), .DLYA0(VSS),
.DLYB1(VDD), .DLYB0(VSS), .STATASEL(VSS), .STATBSEL(VSS));
PWR U1(.Y(VDD));
GND U2(.Y(VSS));
endmodule

```

Integration in an HDL Flow

The integration of the generated PLL module is similar to any VHDL component or Verilog module instantiation in a larger design; there is no special requirement that you need to take into account to successfully synthesize their designs.

For simulation purposes, you need to refer to the VITAL or Verilog library that includes the functional description and the associated timing parameters.

These libraries are available under:

<Designer_Installation_Directory>\lib\vt\95\apa.vhd

<Designer_Installation_Directory>\lib\vlog\apa.v

Optimal Usage of the Global Resources and PLL

Obtaining the Desired Frequencies by Optimizing with Bypass Mode

When the primary and secondary clock outputs are driven by the PLL reference clock, their frequency relationship is given by EQ 6 on page 6. The SmartGen algorithm will attempt to set the first and second dividers so that the requested frequencies will be generated after CLKOUTPLL is divided down by the " $\div u$ " and/or " $\div v$ " dividers. If the exact frequencies cannot be generated for both signals in the given configuration, SmartGen will attempt to satisfy one of the target frequencies. This is not necessarily the primary clock.

Figure 9 and Figure 10 on page 15 illustrate how the bypass mode can be used to obtain a closer frequency match.

Let the input to the PLL be CLK = 40 MHz, and let the target frequencies be GLB = 100 MHz (Primary) and GLA = 13.3 MHz (Secondary).

CASE A

Both primary and secondary clocks are selected with no bypasses. These are the results:

CLKOUTPLL = 53.3 MHz

GLB = 53.3 MHz

GLA = 13.3 MHz

CASE B

Both clocks are selected with the secondary clock bypassed. Note that the input clock is also connected to CLKA. These are the results:

GLB = 100 MHz

GLA = 13.3 MHz ($n = 2$, $m = 5$, $u = 1$ and $v = 3$)

Case B provides the desired results.

Actel Designer tool will not override your bypass setting, even if rerouting the signal may produce a better result.

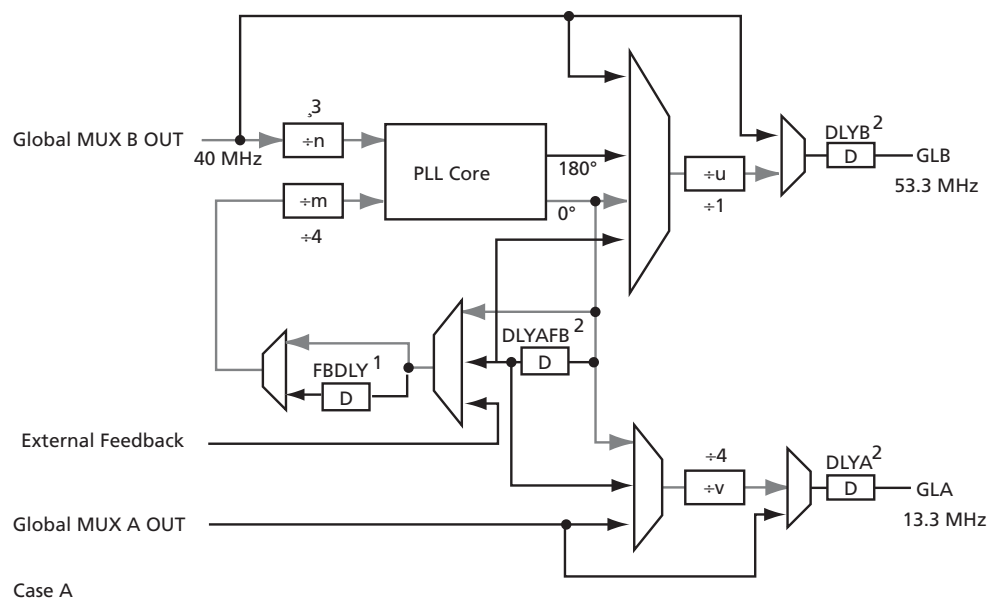


Figure 9 • Using the Bypass Mode to Optimize Target Frequencies – Case A

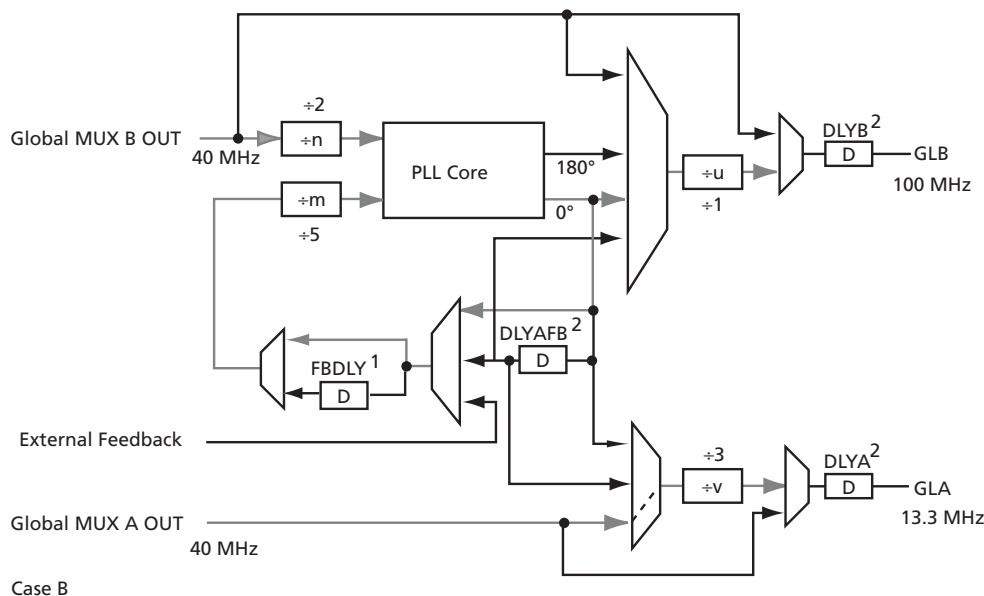


Figure 10 • Using the Bypass Mode to Optimize Target Frequencies – Case B

Selecting the Desired Global Network

In some cases, the designer might want to reassign signals to specific global networks. For instance, you can move a GLINT macro from the east side to the west side in order to reduce source-to-buffer delay. Actel's Designer software represents the global network driver as an I/O pad residing on the east and west part of the I/O ring. The exact pad locations are given in Table 6. A global network driver is a macro that has access to the global resource lines (such as GLINT, PLL, or GL33). Figure 11 on page 16 shows GLINT as the driver of a global line.

To assign a signal to any one of these pads, enter the following in the .gcf file:

```
set_io [pad_name] "instance_name";
```

For example:

```
set_io E 36 "MY_GLINT";
```

where MY_GLINT is the instance name for a GLINT macro in your netlist.

Table 6 • Global Driver Pad Location

Device	East Pads	West Pads
APA075	E 16, E 17	W 16, W 17
APA150	E 32, E 33	W 32, W 33
APA300	E 36, E 37	W 36, W 37
APA450	E 36, E 37	W 36, W 37
APA600	E 52, E 53	W 52, W 53
APA750	E 68, E 69	W 68, W 69
APA1000	E 84, E 85	W 84, W 85

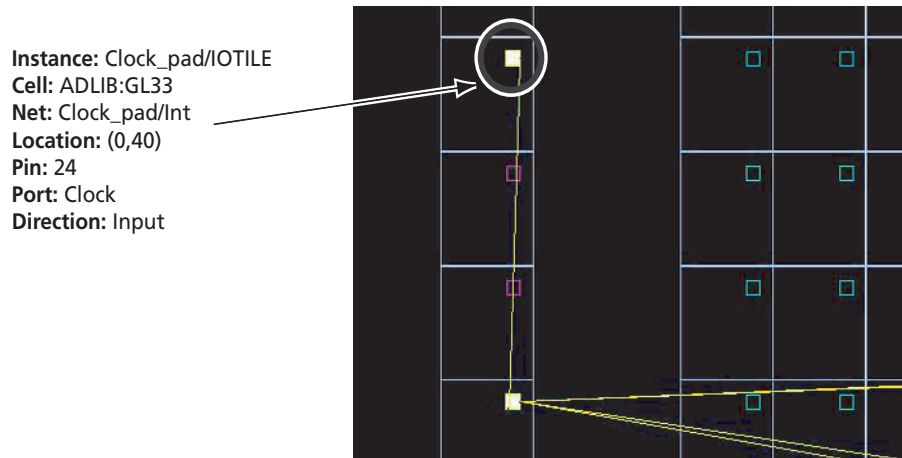


Figure 11 • Examining the Global Network Driver in Actel Designer ChipPlanner

Cascading PLLs

When it is absolutely critical to obtain a clock of the target frequency, phase shift, and delay, you can also employ the second PLL to get a better match to the desired frequency. It should be noted that cascading PLLs cannot be used to exceed the frequency range specifications, and it also adds routing delays.

Place-and-Route Stage Considerations

To reiterate, the ProASIC^{PLUS} clock conditioning circuitry contains the PLL core, the associated dividers, delay elements, and routing MUXes, shown on [Figure 1 on page 2](#). Any signals that are assigned to a global network must pass through the clock conditioning circuitry in order to reach the global network drivers.

Actel's Designer software routes the design based on the macros used, the connections among the macros, and any fixed pins. The placement priority is:

1. The PLLs (bypassed or not) and the GLINT macros are placed first.
2. All constraints set in the .gcf file are treated next.
3. Any remaining GL macros and promoted globals are placed last.

To avoid potential problems, designers should adhere to the following guidelines:

- Limit the design to two global sources per side, whether through an internal signal or an I/O pin.
- Avoid fixing the pins if possible. When compatible macros are chosen, Actel Designer software automatically selects the best pins for the global signals.
- If possible, use IBx and IBxU macros over GLx and GLxU macros, if the PLL is used on the same side of the die. The GL macros will restrict the pin to one of the four GL pins on the device and will use the Global MUX, which is already occupied by the PLL. The IB macros offer greater flexibility. IB input buffers can be assigned to GL pins without driving the global network. To promote the output of an IB input buffer to global, you can exploit the "set_global" command in the GCF file.
- Actel Designer software automatically promotes high fanout signals to globals if resources are still available. It may also demote a signal if a better candidate for the global resource is found. Promoted signals will show in the Compile status report, PinEditor, and ChipViewer as "IBxx/GLxx," whereas demoted signals will show as "GLxx/IBxx." You can set global constraints to manually assign signals if desired.
- No GL-macros should be directly connected to the CLK and CLKA ports of the PLL block with the exceptions of GLINT, GLPE, GLPEMIB. Furthermore, the latter two should not be connected to the CLKA port of any PLL block.

- Due to architectural restrictions, it is not possible to instantiate more than two GLMX macros in the same design. It is also not possible to have more than two LVPECL inputs (GLPE and GLPEMIB macros).
- The EXTFB port is routed to the GLMX pin when external feedback is in use. As such, it is not possible to use any GLMXx or GLMXLx macros on that side. Nor can any internal signals be connected to the EXTFB port.
- Always check the global signal routing in ChipViewer and verify the timing prior to fixing the board layout.
- Do not use GLMX and GL on the same side to drive the PLL input and reference clock. This is not legal.

Poor practices manifest themselves as unexpected and undesirable results in the place-and-route phase of the design. Typically, these can be classified as one of two problems:

- Failure to Compile or Layout

Certain global buffer macros (GL-macros) are designed to output directly onto the global network, so these macros cannot share a side with a PLL block. An error occurs when you attempt to connect such a macro directly to a PLL block or when the displaced macro fails to fit on the other side. Another common cause of this failure is that you mistakenly instantiated too many global signals.

- A long delay as a result of a "Route-around"

When one of the scenarios above results in a displacement rather than a failure, the signal could be moved to another side of the chip. It must then be routed through local connections before it can reach the global network driver, adding delay to the clock signal.

Board-Level Considerations

The analog voltages of the PLL are AVDD and AGND. If the PLL is used, the analog ground can be connected to the system ground, while AVDD should be tied to a noise-free 2.5 V source.

If the design does not use the PLLs, the place-and-route tool disables the PLLs to reduce device power consumption. The board recommendation is to tie the AVDD to a noise-free 2.5 V source and to ground AGND. This recommendation also helps reduce the noise on the board. If the PLLs are used, board layout designers need to be careful with the analog power pins. These pins must be kept free during place-and-route of the design. On the board, designers need to add an RC filter (5 Ω , 200 nF ceramic) in front of the analog power. It is advisable to place the RC filter close to the package pin and minimize inductance on the capacitor, resistor, and traces.

Related Documents

Datasheet

ProASIC^{PLUS} Flash Family FPGAs

http://www.actel.com/documents/ProASICPlus_DS.pdf

Application Notes

ProASIC^{PLUS} PLL Dynamic Reconfiguration Using JTAG

http://www.actel.com/documents/APA_PLLdynamic_AN.pdf

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version 5192688-6/9.07*	Page
5192688-5/12.04	Table 1 • PLL Core General Characteristics was deleted.	N/A
	Figure 1 • Internal Architecture of the ProASICPLUS Clock Conditioning Circuitry was updated to delete the following: <ul style="list-style-type: none"> • 270° and 7 signal • 90° and 5 signals 	page 2
	Table 1 • Clock Conditioning Circuitry Multiplexor (MUX) Settings was updated to change 90° and 270° to Not Used.	page 3
	The Functional Description section was deleted because the content was redundant with the information in the "Clock Division and Multiplication" section.	N/A
	The "Clock Division and Multiplication" section was updated to include information about /u and /v.	page 5
	Figure 4 • Phase Shift of Primary Clock was updated to delete 270° and 90°.	page 7
	The "Phase Shift" section was updated to delete 270° and 90°. Information was also added about phase synchronization between CLKA and CLKB.	page 7
	In "The Primitive Port List" section, Dividers was updated to include OBDIV and OADIV information.	page 10
	In Table 3 • OBMUX [2:0] Global Multiplexing in GLB Path, the descriptions for values 101 and 111 were changed to "Not Used".	page 11
	Figure 8 • SmartGen GUI for PLL Generation was updated with a SmartGen screenshot since the previous one was from ACTgen.	page 12
	Figure 9 • Using the Bypass Mode to Optimize Target Frequencies – Case A was updated to delete 270° and 90°.	page 14
Figure 10 • Using the Bypass Mode to Optimize Target Frequencies – Case B was updated to delete 270° and 90°.	page 15	
5192688-4/06.04	Table 1 was updated.	page 1
	Figure 1 was updated.	page 2
	"Functional Description" was updated.	page 4
	Figure 2 was updated.	page 5
	Figure 7 was updated.	page 11
	Figure 11 was updated.	page 16
5192688-3/09.03	Figure 1 was updated.	page 2
	"Board-Level Considerations" was updated.	page 17

Note: * The part number is located on the last page of the document.

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